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An updated design of the read out link and control board for the Phase-2 upgrade of the ATLAS Tile Calorimeter.

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The ATLAS hadronic Tile Calorimeter (TileCal) is being upgraded for the High Luminosity Large Hadron Collider (HL-LHC). We present a redesign of the TileCal Phase II read out link and control Daughterboard (DB). The DB has a double redundant radiation tolerant design that will provide continuous high-speed readout of digitized data samples of 12 photomultiplier channels each with two gains, while handling the timing, control and communication between the front-end and off-detector electronics, all over multi-gigabit optical links. Four SFP+ modules serve 4×9.6 Gbps uplinks and 2×4.8 Gbps downlinks, handled respectively by two re-programmable Kintex Ultrascale+ FPGAs and two CERN developed gigabit link ASICs (GBTx). Better high-speed uplink timing and improved radiation tolerance have been achieved by migrating the previous design from the Xilinx Kintex-7 FPGAs to the Kintex Ultrascale+ architecture. Preliminary TID radiation tests were performed on a Daughterboard revision 5 following the TOTAL DOSE STEADY-STATE IRRADIATION TEST METHOD ESCC22900 and the ATLAS protocol and safety factors.

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1. The Daughterboard Revision 5 design (DB5)

The DB5 has a double redundant design, allowing nominal running with either one or two working links powered by 4 SFPs+ modules. A 4.8 Gbps link is received by each of the two radiation tolerant GBTx ASICS to recover two 160 MHz good quality LHC synchronized clocks used to drive the transceivers of both FPGAs, and six 40 MHz phase configurable clocks, two of them driving the FPGAs relevant logic and four driving the digitizing blocks of three dual-gain ADC channels each. Each of the two GTY powered Kintex Ultrascale+ FPGAs drive two redundant 9.6 Gbps uplinks. Each FPGA is powered with Triple Modular Redundancy enabled firmware and transmits continuous GBT-CRC protected words with digitized PMT data and detector control information to the back-end.

2. TID tests performed on the DB5

The DB5 was exposed to a total of 20 kRad delivered by a 9 MeV e^- beam in six doses over $\approx$ 1 hour, following the ESCC-22900 standard[2] Level E of TID (20 kRad/200 Gy) "Standard Rate - Window 1": 365 Rad(Si)/min @ 9 MeV and 381 Rad(Si) / min @ 12 MeV. Between doses, the system was power cycled and FPGAs reconfigured from the PROMs. Monitored currents were constant over the full irradiation process, apart from the GBTx which had a small but measurable current decrease after the 20 kRad exposure (Figure 1a). Temperature and current monitoring showed no evidence of latch-up (Figure 1a and 1b). Core FPGA voltages(VCCint) were extremely stable over the entire irradiation period (Figure 1c). The test finished successfully with no component failure on either the board or the two types of SFP+ tested: the CORETEK CT-000NPP-SB1L-D and the AVAGO AFBR-709SMZ.

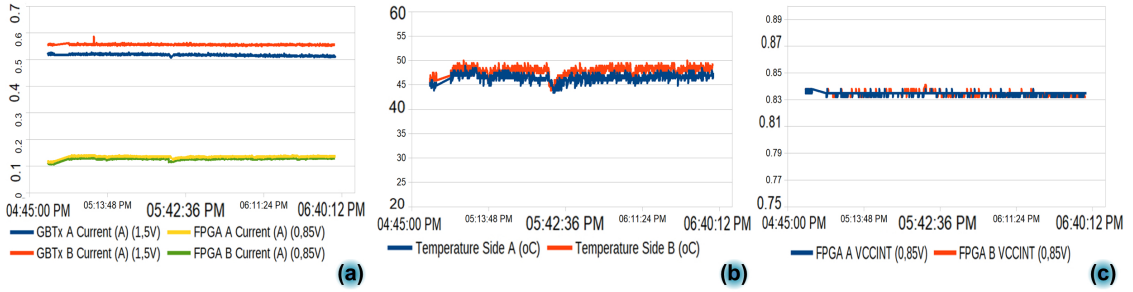

Figure 1: TID Test Results for the DB5 exposed to a total dose of 20 *kRad*.

3. Conclusions

The DB revision 5 was designed to meet all the requirements for the Phase-II Upgrade. The TID radiation tests showed good preliminary results. However, the doses may need to be adjusted to new ATLAS simulation values according to the ATLAS protocol and safety factors.

References

[1] ATLAS collaboration. Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter. CERN-LHCC-2017-019, ATLAS-TDR-028, 2017

[2] TOTAL DOSE STEADY-STATE IRRADIATION TEST METHOD ESCC22900, http://escies.org/escc-specs/published/22900.pdf, 2016.