PROCEEDINGS OF SCIENCE

Front-end Electronics of the Forward Strip Detector for the ATLAS HL-LHC Upgrade

Carlos García Argos[a]*, **Ashley Greenall**[b], **Marc Hauser**[a], **Karl Jakobs**[a], **Kambiz Mahboubi**[a], **Ulrich Parzefall**[a], **Liv Wiik-Fuchs**[a] **and Sven Wonsak**[b]

[a] *Physikalisches Institut, Albert-Ludwigs-Universität Freiburg*
Freiburg-im-Breisgau, Germany
[b] *Oliver Lodge Laboratory, University of Liverpool*
Liverpool, United Kingdom
E-mail: carlos.garcia.argos@physik.uni-freiburg.de

The ATLAS Experiment will upgrade its central tracking detector with an all-silicon Inner Tracker (ITk) for the HL-LHC, comprising pixel and strip detectors. The strip detector is based on silicon strip sensors, which are read out by low mass, radiation hard circuits carrying custom designed radiation hard ASICs in 130 nm technology. The circuits are made from flexible PCB multi-layer copper polyimide constructions. The ASICs are glued onto the flex and connections are made by wire-bonding. This contribution discusses the evolution and electrical performance of various hybrid prototypes necessary to equip the forward region of the detector, as well as their final development.

Topical Workshop on Electronics for Particle Physics (TWEPP2018)
17-21 September 2018
Antwerp, Belgium

*Speaker.

PoS(TWEPP2018)014

1. Introduction

The ATLAS Experiment [1] will upgrade its tracking system for the High Luminosity LHC (HL-LHC) in 2024, using an all-silicon Inner Tracker (ITk). This contribution focuses on the forward strip detector, which is made from petals, structures onto which detector modules are mounted. They provide cooling, mechanical support and power to the modules. The detectors are arranged in six rings, named from 0 to 5, covering different widths and occupancy regions by having sensors with different strip lengths and numbers. A schematic view of a petal is shown in Figure 1 [2].

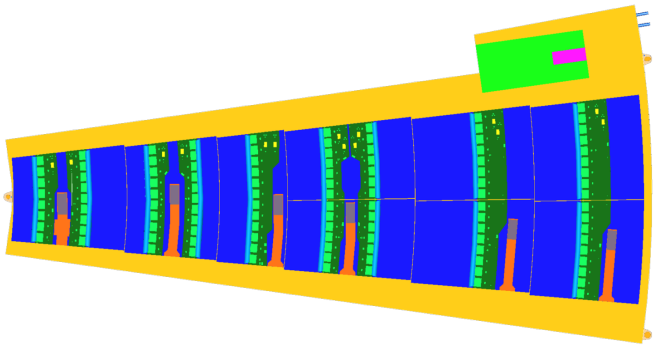

Figure 1: Sketch of an end-cap petal showing the six different rings, named 0 to 5 from left to right.

The sensors are read out by analogue front-end chips, which are named ABC (ATLAS Binary Chip) and produced in a 130 nm CMOS process [3]. The digital front-end chip, named Hybrid Controller Chip (HCC), sends control commands to the ABCs and aggregates the data from the ABCs to send it to the DAQ. The prototype chips are named ABC130 and HCC130, whereas the production chips are named ABCStar and HCCStar. Prior prototypes were developed using chips produced in a 250 nm CMOS process [4].

This contribution covers the construction and testing of the prototypes for rings 0, 1, 3, 4 and 5, as well as all the rings of the production hybrids. The experience in the design, manufacture and testing of the prototype hybrids and the design status of the production hybrids is presented.

2. Design and Testing of Prototype Hybrids

Because of the geometry of the end-cap sensors, the hybrids that read out the different sensors differ for each ring. The maximum number of ABCs that an HCC can read out is 11, while some portions of the rings hold up to 18 chips, which implies that the number of HCCs has to be increased in some areas. Tables 1 and 2 show the ABC and HCC distribution for each of the hybrid types.

In addition, due to the use of 6-inch wafers to produce the sensors for the tracker, the module for rings 3, 4 and 5 are split into two parts. This leads to two sensors side by side and a stitching area between the hybrids, which transmit power and data from one side of the module to the other.

The first number (after "R") denotes the ring where the hybrid is. For most rings there is more than one hybrid. The second number (after "H") denotes the position of the hybrid in the module.

Hybrid	R0H0	R0H1	R1H0	R1H1	R2H0
HCCs	1	1	1	1	2
ABCs	8	9	10	11	12

Table 1: List of end-cap hybrid types and the number of HCCs and ABCs for the non split module region.

Hybrid	R3H0	R3H1	R3H2	R3H3	R4H0	R4H1	R5H0	R5H1
HCCs	0	2	0	2	0	2	0	2
ABCs	7	7	7	7	8	8	9	9

Table 2: List of end-cap hybrid types and the number of HCCs and ABCs for the split module region.

In non-split modules (rings 0, 1 and 2), "H0" means the hybrid is in the position closer to the beam pipe and "H1" is for the hybrid furthest from the beam pipe in that module. In split modules (rings 3, 4 and 5), "H0" or "H2" is the hybrid to the right and "H1" or "H3" is the hybrid to the left.

2.1 Hybrid Fabrication and Assembly

The hybrid PCBs are fabricated in industry using four copper layers (two power planes and two signal planes) on polyimide, resulting in a flexible circuit with minimal mass. Track width and gap are 100/100 µm and vias are laser-drilled through-hole or blind. All through-hole vias are covered in order to avoid glue seepage in the ASIC attachment process. The target thickness of the PCB is 300 µm $\pm$ 10% and the typical measured thickness is around 275 µm.

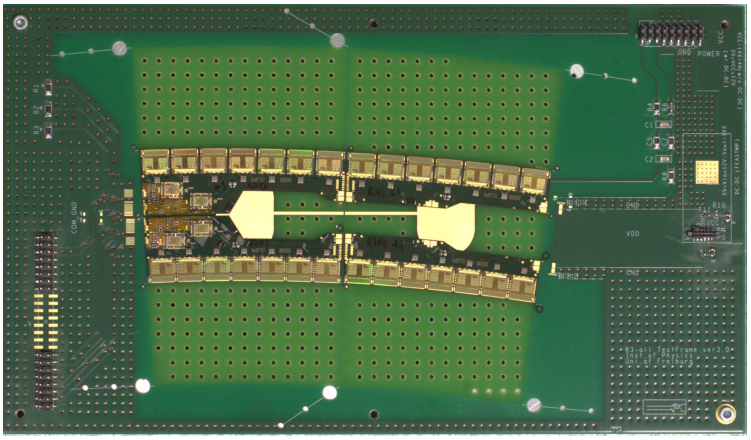

Figure 2: An end-cap set of Ring-3 hybrids on their test board. The four rectangular chips on the left-hand side of the hybrids are the HCCs and the ABCs are visible as square chips spread along the hybrids.

The PCBs are populated with passive components at the University of Freiburg. Ultraviolet curable glue is dispensed using an automated dispenser and dedicated tooling, produced in-house, is used to precisely position the ASICs and control the glue thickness, holding them during the glue curing process. Curing is achieved by illuminating with ultraviolet LEDs for 120 seconds. Last, the electrical connections are made by automated wire-bonding and the hybrids are also wire-bonded

onto a test board that allows the use of standard connectors to power and read out the hybrids. Fiducial markers added to the PCB top layer are used by the pattern recognition systems of the wire-bonding machines to facilitate the automated bonding process.

Figure 2 shows a picture of Ring-3 hybrids on the testing board in the positions in which they would be glued onto the sensors. The stitching area is visible between the hybrids.

2.2 Electrical Tests

Characterisation of the hybrids is done by two main analogue tests: response curve and noise occupancy, which give their performance in terms of input noise and noise occupancy. A detailed description of these tests can be found in Ref. [5].

Figure 3 shows the noise occupancy test result for hybrid R4H1. Figure 4 shows the input noise results for hybrid R5H0. The results are equivalent for all hybrid types and compatible with the expectation from the chip designers, around 450 e^-ENC. The gap in the channel count is caused by the the software, which counts the chips from the minimum to the maximum address and then books histograms for the full range. The end-cap hybrids use non-consecutive addresses, hence the gap.

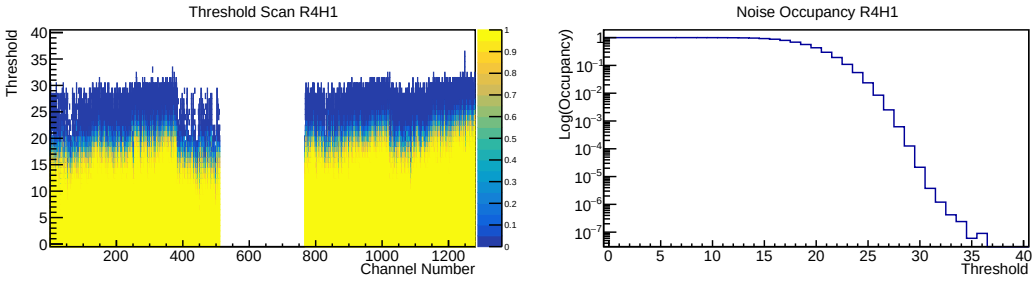

Figure 3: Noise occupancy of hybrid R4H1. The left plot shows the threshold scan for all channels and the right one shows the projection for the whole hybrid.

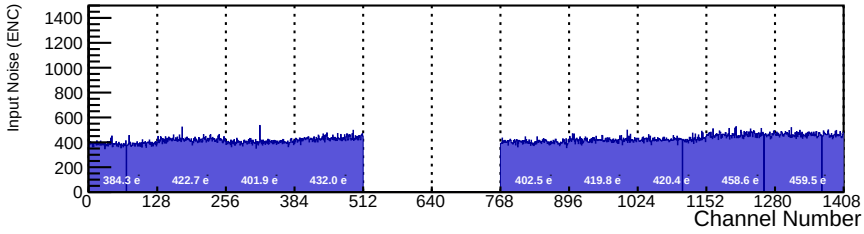

Figure 4: Input noise of hybrid R5H0.

3. Star chipset: From Prototyping to Production

The production chips will change the digital read-out architecture. The ABC130/HCC130 chipset has a daisy chain read-out, in which the data from the ABC130 chips are sent to the neighbour and the last ABC130 in the chain forwards all the data to the HCC130. By contrast, the ABCStar chips have a point-to-point connection to the HCCStar chip. Both are shown in Figure 5.

This poses an additional challenge for the PCB routing, particularly for highly populated hybrids. The Ring-2 hybrid, shown in Figure 6 is the longest one, with 12 ABCStar and 2 HCCStar chips, for a total of 12 sets of data lines in a limited amount of space.

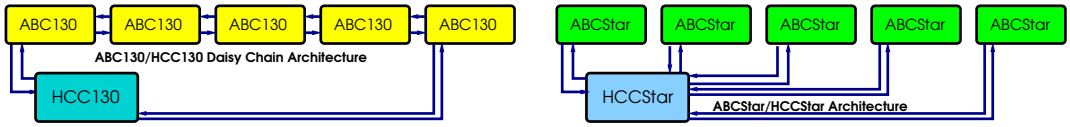

Figure 5: Read-out architectures of the ABC130 chips from the HCC130 chip and of the ABCStar chips from the HCCStar chip.

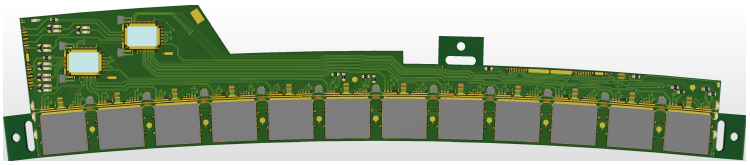

Figure 6: Layout of the Ring-2 hybrid for the Star chipset.

4. Conclusions

The prototyping phase of the ITk Strip detector read-out hybrids was successful. All hybrid types for the end-cap region performed as desired and as predicted by the simulation of the chips. The design of the production hybrids is also well advanced and the first hybrids should be available near the date of availability of Star chips, before the end of 2018.

5. Acknowledgements

The authors acknowledge the contributions of Peter Phillips, Craig Sawyer, Bruce Gallop and Matthew Warren. This work has been supported and financed by the Federal Ministry of Education and Research (BMBF, Germany) and the Science and Technology Facilities Council (STFC, UK).

References

[1] ATLAS Collaboration, "The ATLAS Experiment at the CERN Large Hadron Collider," JINST **3** (2008) S08003. doi:10.1088/1748-0221/3/08/S08003

[2] ATLAS Collaboration: Technical Design Report for the ATLAS Inner Tracker Strip Detector. CERN-LHCC-2017-005, April 2017.

[3] J. Kaplon and M. Noy, *Front end electronics for SLHC semiconductor trackers in CMOS 90 nm and 130-nm processes*, IEEE Trans.Nucl.Sci. 59 (2012) 1611-1620.

[4] K. Mahboubi *et al.*, "The front-end hybrid for the ATLAS HL-LHC silicon strip tracker," JINST **9** (2014) C02027. doi:10.1088/1748-0221/9/02/C02027

[5] C. García-Argos *et al.*, "Assembly and Electrical Tests of the First Full-size Forward Module for the ATLAS ITk Strip Detector," HSTD&SOIPIX2017, doi:10.1016/j.nima.2018.09.082