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A 1 GS/s sampling digitizer designed with interleaved architecture (GSPS) for the LaBr3 detectors of the FAMU experiment.

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A fast continuous sampling digitizer has been designed to acquire fast scintillating detector signal from cerium activated lantanum bromide ($LaBr_3(Ce)$) scintillation crystal. These are foreseen in the FAMU experiment which is aimed at spectroscopic measurements of muonic hydrogen, possibly providing insights into the so-called proton radius puzzle. The board, named GSPS, is implemented as an FMC mezzanine which hosts two off-the-shelf sampling ADC used in interleaved timing architecture, achieving a 1 GS/s sampling rate (with a 12-bit nominal accuracy over the first Nyquist interval of frequencies, ranging from DC to 500 MHz). Interleaved technique allowed us to keep both lower production costs and simple acquisition system avoiding complex interface protocols like JESD204. The board will be described; the test setup and the used methodology to characterize the device will be explained; the achieved performances will be shown and discussed. In particular it will be pointed out how the two interleaved ADCs can be calibrated in order to get the best performance. The different contributions to both noise and distortion affecting the device will be analyzed applying general techniques for high-sampling-speed continuous ADCs. Lastly, future improvements will be introduced: in particular, the solutions we foresee to get a effective number of bits of about 10 over the whole first Nyquist interval will be enlightened.

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1. Introduction

The Bologna Division of INFN and the Physics Department of the University of Bologna are developing X-rays detectors for the FAMU project, a nuclear spectroscopic experiment that is planned to measure physics properties of the muonic atom. The detectors are made of Lanthanum bromide scintillating crystals [LaBr3(Ce)] coupled with a high quantum efficiency photomultiplier. Fast sampling electronics is currently under development; it should be able to acquire a sufficient number of samples of the detector signal waveform to guarantee the desired energy and timing resolution. The current preliminary acquisition system consists of commercial devices sampling at 500 MSample/s. In this paper we present a prototype of a 1 GS/s digitizer based on two off-the-shelf ADCs with an interleaved architecture. In section 2 the FAMU experiment will be introduced and the requirement on the electronics will be enlightened as well. The digitizer will be described in 3. The methodology and the setup we used to test it will be presented in 4 whilst the achieved performance will be discussed on 5. In the last section (6) we will describe the future improvements that are foreseen on the next prototype in order to achieve better performance.

2. The Famu Experiment

The FAMU (*Fisica degli Atomi MUonici*) project is an experiment aimed at performing a spectroscopic measurement of the hyperfine transition of the muonic hydrogen 1S state. This will lead to the best resolved proton Zemach radius estimation, possibly providing insights into the so-called proton radius puzzle[1]. The proposed experimental method is described in [2] where the results of preliminary tests performed with the RIKEN-RAL facility located at the Rutherford Appleton Laboratory (U.K.) in June 2014 are shown as well. Muonic hydrogen atoms (μ p) are formed by a pulsed muon beam interacting with hydrogen gas target. The hyperfine transition of the μ p ground state is induced by a mid infrared tunable source. By adding small quantities of oxygen to hydrogen it is possible to observe the number of hyperfine transitions which take place, measuring the time distribution of the X-rays emitted from the muon-transfer events to the added gas. Detection of this characteristics X-rays is performed using scintillating counters based on $LaBr_3$(Ce) crystals (energy resolution ~3% at 662 keV and timing resolution < 600 ps) read out by Hamamatsu R11265-200 PMTs. Description of the detector can be found in [3] where the performance was studied with a ditigizer, designed to provide a 14-bit, 500 MS/s analog to digital conversion. Time and energy of the X-rays will be reconstructed on-line by processing the detector digitized waveforms.

3. The 1 GS/s digitizer prototype

In order to achieve better energy resolution, a new digitizer, called GSPS, has been designed. Simulation studies suggested that a high resolution ($\geq$ ~9 of effective number of bits) and high rate (1 GS/s) sampling allows the signal waveform to be reconstructed without reducing the crystals energy resolution (~3%). Continuous sampling is also essential to perform on-line digital processing for monitoring both target and detector performance. Moreover, low cost and ease of use are preferred options thus, the adoption of off-the-shelf components and low complexity solution are

favoured. Most of high speed off-the-shelf digitizers (sampling with more than 10 bit) are using only JESD204 to cope with the high output data rate. To reduce firmware design complexity, we decided to not use it for this prototype. We chose a standard parallel bus which was easier and faster to implement on FPGA. Moreover, we favoured dc-coupling with the detector in order to better cope with pile-up effects. To meet requirements, we implemented the GSPS digitizer with two Analog Devices AD9434 ADCs in timing interleaved architecture, both of them running at 500 MS/s but with opposite clock phase. The first prototype is host by a 6-layers PCB, FMC-form mezzanine card (see picture 1). The ADC AD9434 is 12-bit resolution, with a typical input range

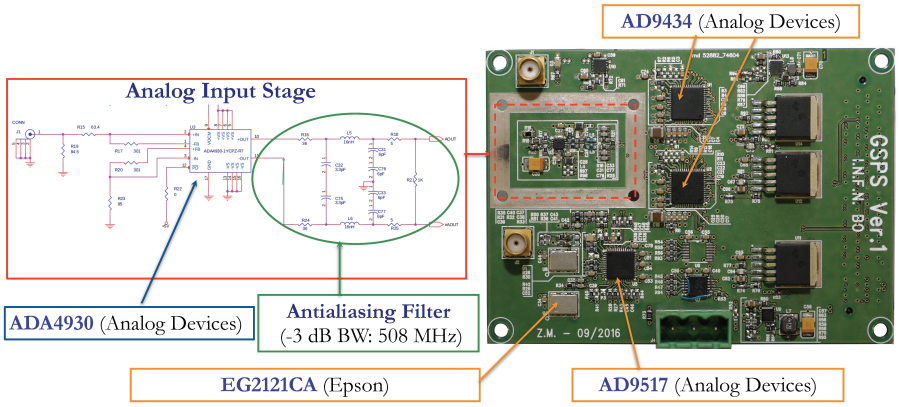


Figure 1: Picture of the GSPS digitizer. The analog input stage is schematized on the left.

of 1.5 V_{pp} , effective number of bits (ENOB) of 10.5, SNR = 65 dBFS. Digitized data are transmitted thanks to a LVDS parallel bus. The clock is generated by a 500 MHz LVDS-output oscillator (phase jitter from 12 kHz to 20 MHz = 300 fs, total RMS jitter = 3 ps [1]) distributed to the ADCs through the Analog Devices AD9517; even if this is a clock generator with internal VCO, it is used only as a buffer thanks to the already low jitter performance of the oscillator. The input of GSPS is a single-ended signal, fed into a low noise fully differential amplifier (ADA4930) which has a -3dB bandwidth of 1.35 GHz, a typical noise of 1.2 nV/$\sqrt{Hz}$ and low harmonic distortion (HD2 @100 MHz = -73 dBc).

4. Test methodology

In order to perform tests and measure GSPS performance, the mezzanine card has been plugged on the FMC connector of an off-the-shelf motherboard (see picture 2), called ZedBoard[2] based on Xilinx Zynq-7000 FPGA. A dedicated firmware has been designed by developing an ad-hoc IP core with the Xilinx Vivado software. Dynamic performance measurements are performed using a

[1] Clock jitter degrades ADC performance. Its contribution can be guessed by two factors: phase noise close to the first harmonic (high contribution over a narrow frequency range) and the floor (low contribution in magnitude but integrated over the whole analog bandwidth of the device). In this specific case, the total RMS jitter on the clock oscillator datasheet were measured with an instrument having a bandwidth greater that 2 GHz. AD9434 clock input pin is specified to have a bandwidth of about 1 GHz, so an ëffectiveëjitter of less than 1.5 ps is expected. This should meet requirements at least up to an input signal bandwidth of about 200 MHz.

[2] www.zedboard.org

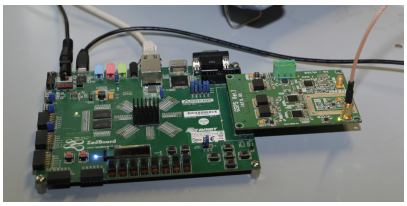


Figure 2: GSPS test setup.

Figure 3: 5-cells Butterworth low pass filter.

Rhode & Schwarz RF signal generator (SMB 100A) with custom low-pass filters to suppress the higher harmonics (see fig. 3. As a reference, a Texas Instruments evaluation module (ADS54J60, with a 16 bit, 1 GS/s ADC) has been used to characterize the signal from the generator. Static performance has been measured using a Source Meter (Keithley 2636B) which has a typical noise of 50 μV (0.1 Hz to 10 Hz) and adding a low-pass filter (-3dB bandwidth of ~100 Hz).

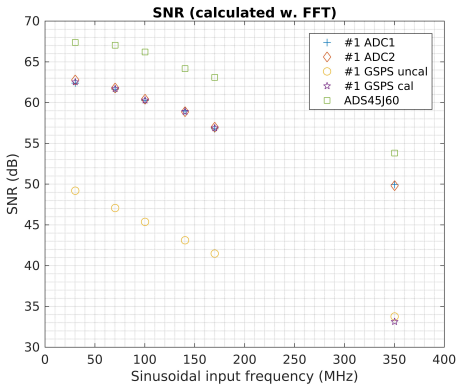
5. Test results

As a first step, the ADCs mismatches have to be measured. A definite input tone has been applied to the GSPS and a 3(4)-parameter least-square fit to sine wave ([4]) performed for every ADC separately. One of the two ADC has been taken as a reference and the second one corrected by using the mismatches measured by the reconstructed sine waves[3]. The offset mismatch has been corrected by summing the offset found.The bandwidth mismatch has been compensated with a 11-tap digital FIR filter with variable gain. The timing mismatch has been corrected with a 21-tap digital FIR Fractional Delay filter.Because filter are applied on a single ADC sample, this approach has found to be effective up to a bandwidth of 250 MHz. The performance of the calibrated GSPS have been evaluated by measuring the SIgnal-to-Noise And Distortion ratio (SINAD) as a function of the frequency (see table 1). SINAD contributions are: quantization and analog noise (frequency independent), clock jitter noise and harmonic distortion. The first three contributions can be extracted from the Signal to Noise Ratio (SNR) plot 4a. The low frequency region is particularly affected by quantization and analog noises (~63 dB); this is confirmed by the random noise obtained from static measurement (~63.3 dB). From the SNR, the clock jitter contribution can be determined by evaluating its frequency dependance: a RMS jitter of 1.18 ps is measured; the corresponding contribution to the SINAD is, for instance, 59 dB at 150 Mhz. The harmonic distortion is found to be dominant at frequency greater than 150 MHz (fig. 4b); the fully differential amplifier is the main source of this effect.

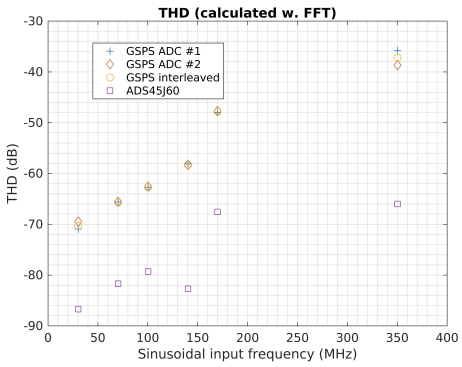
6. Conclusions and future perspectives

The first prototype of a 1 GS/s digitizer for the FAMU experiment has been designed with a timing interleaved architecture. A solid method to calibrate the digitizer has been shown and its performance has been evaluated. The measured ENOB is close to the goal of ~10 up to a frequency of about 100 MHz; main noise contributors have been identified and they will be mitigated in the next upgraded prototype to reach better performance. First, a differential amplifier with lower

[3]Correction are implemented off-line with MATLAB



(a) Signal-to-Noise Ratio



(b) Total Harmonic Distortion

Figure 4: GSPS Noise performance as a function of the frequency of the input sinusoidal tone. Data are plotted independently for each ADC (#1 and #2), for GSPS interleaved sampling (calibrated data are visible on both plots and uncalibrated only in 4a) and for Texas Instruments ADS54J60 reference.

Frequency (MHz)	**SINAD** (dB)	**ENOB**
30.3	61.86	9.98
70.3	60.24	9.71
100.3	58.34	9.40
140.3	55.57	8.94
170.3	47.32	7.57
350.3	31.68	4.97

Table 1: Measured performance of the calibrated GSPS in term of Signal-to-noise and distortion ratio (SINAD) and effective-number of bits (ENOB).

harmonic distortion at frequencies greater than 150 MHz is mandatory; then, a pair of clock source and buffer with lower jitter are preferred (to reduce noise around ~100 MHz). Mismatch calibration amongst ADCs must be mitigated: the adoption of ADCs whit internal fine delay on the clock is a viable solution. Advanced filtering techniques to compensate mismatches will be investigated as well. Eventually, calibration digital filters have to implemented on FPGA and the improvement on the detector energy resolution must be measured.

References

[1] R. Pohl et al. *The size of the proton*, *Nature* **466** 213-216 (08 July 2010).

[2] A. Adamczak et al. *Steps towards the hyperfine splitting measurement of the muonic hydrogen ground state: pulsed muon beam and detection system characterization*, *JINST* **11** P05007 (2016)

[3] G. Baldazzi et al. *The $LaBr_3(Ce)$ based detection system for the FAMU experiment*, *JINST* **12** C03067 (2017)

[4] *IEEE standard for terminology and Test Methods for Analog-to-Digital converters*, IEEE Std 1241-2000 2011.