PROCEEDINGS OF SCIENCE

ATLAS Tile Calorimeter Link Daughterboard.

Eduardo Valdes Santurio[1]*, **Samuel Silverstein**[2] **and Christian Bohm**[3]
[123]**Stockholm University**

E-mail(s): [1]eduardo.valdes@fysik.su.se, [1]eduardo.valdes@cern.ch,
[2]silver@fysik.su.se, [3]bohm@fysik.su.se

We have developed an updated Daughterboard design for control and readout of the upgraded ATLAS Hadronic Tile Calorimeter electronics for HL-LHC. In the new design, four SFP+ modules handle: 4×9.6 Gbps uplinks operated by two Kintex Ultrascale+ FPGAs, and 2×4.8 Gbps downlinks operated by two GBTxs. The uplink sends continuous high-speed readout of digitized PMT samples, while the downlink receives control, configuration and LHC timing. Triple Mode Redundancy (TMR), Forward Error Correction (FEC) and CRC (Cyclic Redundancy Check) strategies, plus a double redundant design with radiation tolerant components, minimize single failure points and improves resistance to single-event upsets caused by hadronic radiation. Preliminary TID and NIEL tests were performed following the ATLAS policy on radiation tolerant electronics and those specified in the European Space Components Coordination specification 22900 (ESCC-22900).

Topical Workshop on Electronics for Particle Physics (TWEPP2018)
17-21 September 2018
Antwerp, Belgium

*Speaker.

PoS(TWEPP2018)024

1. Introduction

The ATLAS detector (Figure 1a) is undergoing upgrade work to face the challenges posed by the High Luminosity Large Hadron Collider (HL-LHC). The ATLAS Tile Calorimeter (TileCal) is a sampling calorimeter composed of plastic scintillator tiles as active material, interleaved with steel plates as absorber. TileCal comprises four cylindrical barrels (Figure 1b) each divided into 64 wedge-shaped modules (Figure 1c). Light from both sides of each pseudo-projective cell is collected by wavelength shifting fibers and read out by two photomultiplier tubes (PMTs).

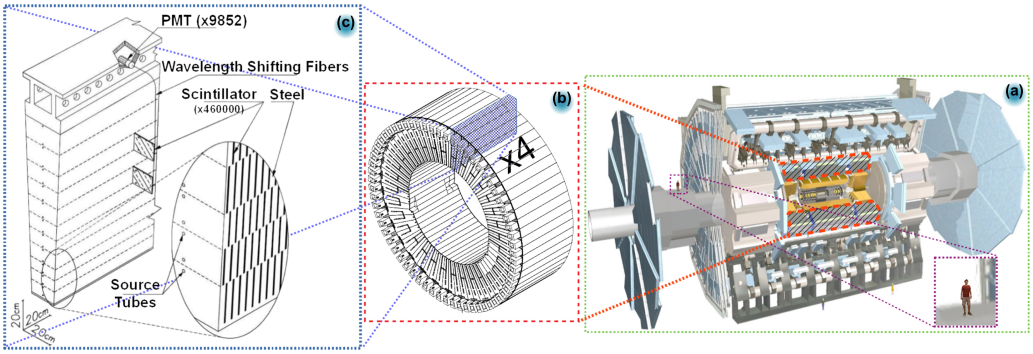

Figure 1: (a) The ATLAS detector. (b) A TileCal barrel. (c) Depiction of a TileCal wedge-shaped module.

The increased luminosity achieved by the HL-LHC will leave the ageing ATLAS Tile Calorimeter (TileCal) electronics unsuited to handle the anticipated higher radiation levels and increased pileup. TileCal's Phase-II upgrade plan intends to assure better timing and energy resolution whilst decreasing the sensitivity to out-of-time pileup[1]. The proposed new design includes on-detector modules that will provide continuous read-out of full-granularity digital data to the off-detector systems through multi-Gbps optic fibers, allowing digital trigger tower summation for better trigger performance. We have designed a radiation tolerant read-out link and control board (Daughterboard) powered by multi-Gbps optic transceivers that will interface the on- and off-detector system. The upgrade R&D work requires Total Ionizing Dose (TID), Non Ionizing Energy Loss (NIEL) and Single Event Effects (SEE) tests to be performed on the updated design of the Daughterboard (DB), in order to qualify it as reliable for the HL-HLC radiation environment.

2. The Phase-II read-out system

TileCal's Phase-II read-out system is modularized in Minidrawers (MD) (Figure 2a), which will sit in the wedge girders and serve up to 12 channels each. The PMT signal is split into 2 channels, with different gains, which are shaped and conditioned by a Front-End Board (FEB) before they are digitized in a Mainboard (MB)(Figure 2b). A DB provides LHC synchronized timing, control and configuration to the Front-End, and continuous readout of the MB channels to the off-detector systems (Figure 2c). A Tile Preprocessor (TilePPr) receives and stores two gains of PMT data in pipelines until a trigger decision event is received, and in parallel provides reconstructed data to the trigger system.

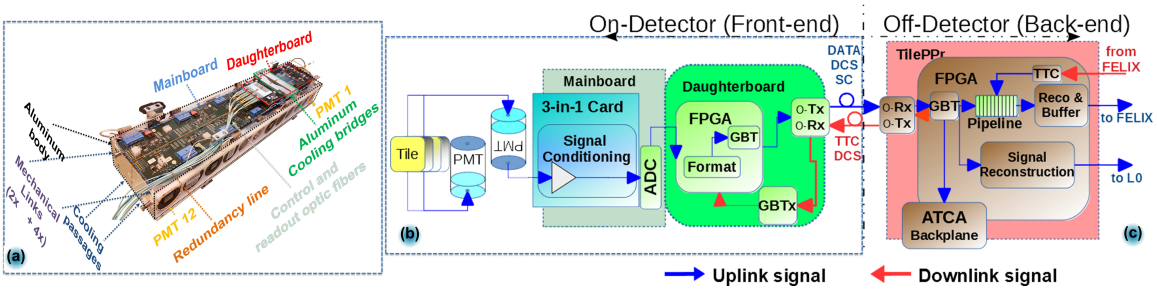

Figure 2: TileCal Phase-II Upgrade read-out system: (a) TileCal Phase-II Upgrade Minidrawer, (b) On-Detector Electronics block diagram and (c) Off-Detector electronics block diagram.

3. The Daughterboard Revision 5 design

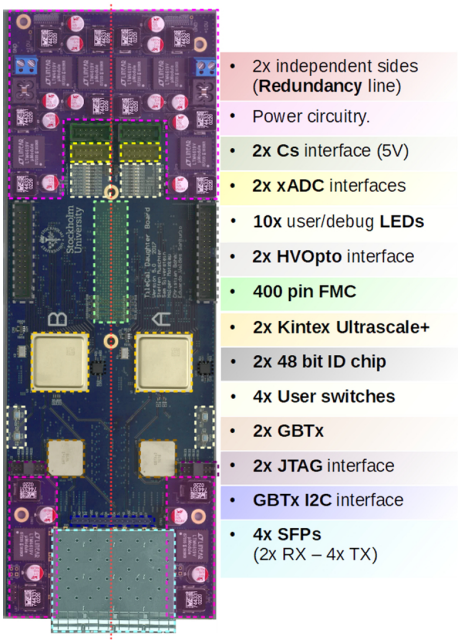

Figure 3: The Daughterboard revision 5.

The DB Revision 5 (DB5) (Figure 3) is designed to minimize single-point failure modes; each side is independently powered, with redundant input and output links. The design is compatible with interfaces from previous designs,including high voltage control, the MB interface, and the Cs calibration system[2]. Additionally, the design includes new digital unique ID serial chips for DB identification on-detector, and an xADC panel per side for external sensor monitoring capabilities.

The interface with the off-detector systems is via two RX and four TX optical fibers connected to four SFP+ modules, with nominal running possible with only one RX and two TX links active. For the downlink, two RX links running at 4.8 drive a pair of CERN GBTx ASICs[4]. Each GBTx chip recovers a set of eight LHC synchronized clocks: 2×160 MHz clocks to drive the transceivers of both FPGAs, 2×40 MHz clocks to drive the FPGAs relevant logic, and 4×40 MHz phase configurable clocks to drive the digitizing blocks on each MD quadrant. Moreover, each GBTx distributes synchronous and asynchronous control and configuration commands to both FPGAs by means of dedicated ports (EPorts) via a configuration bus, while providing off-detector control of both FPGA reset signals and JTAG chains for remote reconfiguration of the FPGAs and their respective attached PROMs. For the uplink, two gains of digitized PMT data and SC information are formatted in GBT-CRC protected words by Triple Modular Redundancy protected FPGA firmware, and continuously transmitted to the back-end through two redundant readout links running at 9.6 Gbps each.

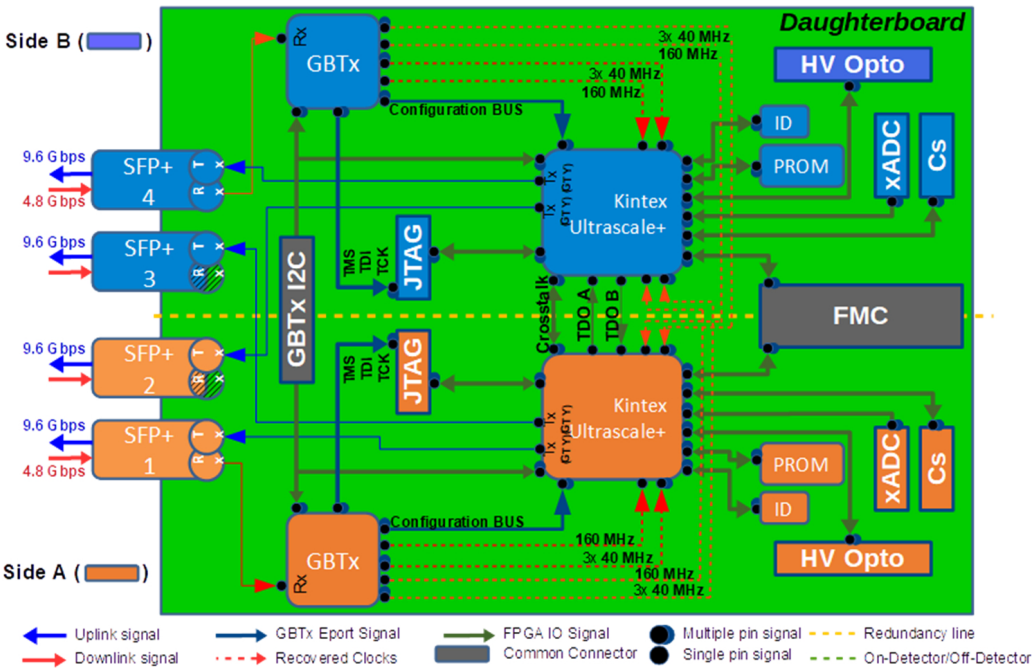

Figure 4: Daughterboard revision 5 block diagram.

4. Preliminary TID and NIEL radiation tests

The DB will be situated within TileCal where relatively high radiation exposure is expected to take place [3], requiring the DB5 to be certified to withstand 20 kRad of Total Ionizing Dose and a total Non-Ionizing Energy Loss corresponding to 1.13×10^{12} - 1 MeV equivalent neutron fluence over the HL-LHC lifetime. Both tests were done following the European Space Components Coordination specification 22900 (ESCC-22900) [5] and the ATLAS policy on radiation tolerant electronics.

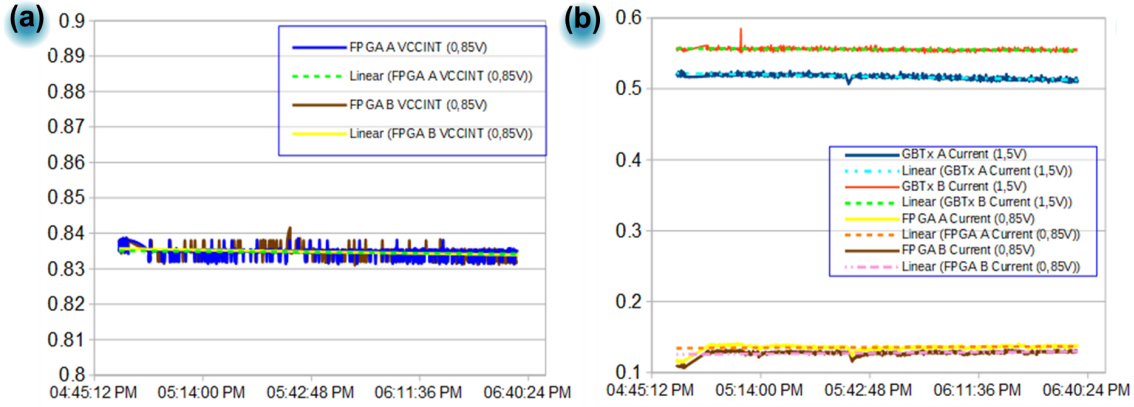

Figure 5: Daughterboard revision 5 TID test results for a board exposed to a total dose of 20 kRad.

The TID test was performed with a DB5 with operative firmware connected to a TilePPr. The board was exposed to a total of 20 kRrad delivered by a 9 MeV e^- beam in six doses over 1

hour. The transceivers powered two pairs of different SFP+ types during the test: CORETEK CT-000NPP-SB1L-D (baseline) and AVAGO AFBR-709SMZ. The test corresponded to a ESCC-22900 Level E of TID with an standard rate of 365 Rad(Si)/min for the 9 MeV and 381 Rad(Si) / min for 12 MeV. The system was power cycled after each dose and FPGAs were reconfigured from the attached PROMs. The FPGA Voltages and currents monitored remained stable over the full dose for the whole board, aside from GBTx currents which had a small but measurable decrease that did not affect the board functionality (Figure 5a and 5b). The PROMs were read out after every dose showing no data corruption, and remained programmable after the 20 kRad dose. The test was finished successfully with no component failures.

NIEL tests were performed with a quasi-monoenergetic 52 MeV proton beam, aimed to achieve a total NIEL dose corresponding to 9×10^{12}/ cm^2 - 1 MeV equivalent neutron fluence. The board was irradiated in two steps following a double-Gaussian beam profile. The Gaussians were 14.8 cm apart in order to achieve a dose homogeneity of around 10% over 21 cm along the redundancy line (Figure 6). In a power-up test immediately after irradiation, both FPGAs and GBTx failed with severe over-currents. After the board cooled down, the GBTxs and the FPGAs were severely damaged with both their VCC and ground being shorted. The AVAGO AFBR-709SMZ microcontroller also died, however the irradiated CORETEK SFP+ transceiver continued to function with no apparent degradation.

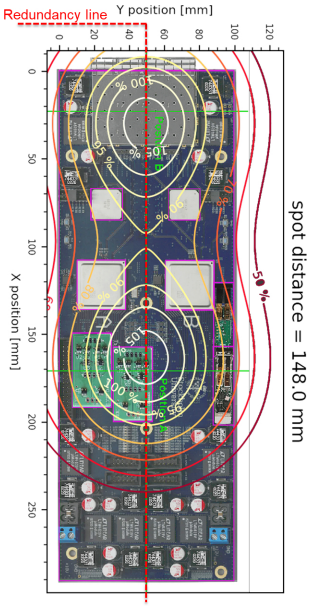

Figure 6: Daughterboard revision 5 NIEL test. 100% dose corresponds to the nominal target dose of 9.694 kGy or 9.00×10^{12}/ cm^2 - 1 MeV neutron equivalent fluence.

5. Conclusions

The DB5 design aims to meet all the HL-LHC requirements. The board successfully passed the preliminary TID radiation tests, however the NIEL tests could only qualify the CORETEK SFP+ transceiver. New NIEL tests are planned using neutrons instead of protons to reduce the ionizing dose. Meanwhile, firmware development and improvement and integration into the MDs is taking place.

References

[1] ATLAS collaboration. Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter. CERN-LHCC-2017-019, ATLAS-TDR-028, 2018

[2] S. Muschter Readout link and control board for the ATLAS TileCal upgrade. DiVA: 805818, 2015.

[3] H. Åkerstedt, A radiation tolerant Data link board for the ATLAS TileCal upgrade, DiVA:921061, 2016.

[4] GBTX Manual, https://espace.cern.ch/GBT-Project/GBTX/Manuals/gbtxManual.pdf, 2016.

[5] TOTAL DOSE STEADY-STATE IRRADIATION TEST METHOD ESCC22900, http://escies.org/escc-specs/published/22900.pdf, 2016.