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A Delay Locked Loop for Time-to-Digital Converters with Quick Recovery and Low Hysteresis

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This paper proposes the simulation results of a 1 GHz Delay Locked Loop (DLL) designed in a 65 nm CMOS technology. The circuit was designed for harsh environments, in particular ionizing radiation. A novel phase detector consisting of an improved bang-bang phase detector and a 3-state controller was introduced, leading to a a single event recovery time of less than 1 us. The DLL is used inside a Time to digital converter, and achieves an in lock hysteresis of only 500 fs.

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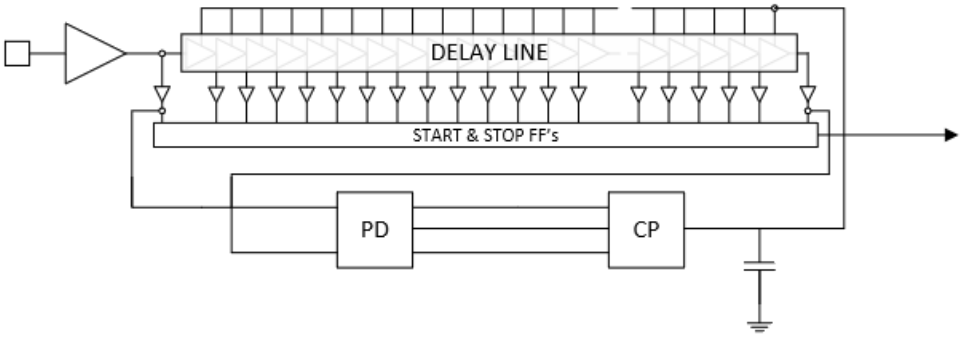

Figure 1: DLL based TDC block diagram.

1. Introduction

Time-to-digital converters (TDCs) have recently gained interest due to technology scaling and the need for more accurate time measurements. With decreasing transistor dimensions, the power supply voltage also decreases, which limits the dynamic range of Analog-to-Digital Converters (ADCs). One solution to this problem is to digitize an analog time instead of a voltage and move from ADCs to TDCs [9].

TDCs have proven to be useful in a lot of applications, like time of flight (ToF) measurements and high-energy physics [1]. Furthermore, a TDC can be used to digitize the phase error of an oscillator in all-digital synthesizers. In this paper, a radiation tolerant TDC is proposed, which can be used in harsh environments [2] [3] [4]. The TDC is designed in 65 nm CMOS and has a resolution of 8 ps. The timing generator delay line is controlled by a delay locked loop (DLL) in order to compensate for possible external influences like temperature, ageing and radiation and to cope with intrinsic process variability [5].This paper is organized as follows: Firstly the different blocks of the analog front-end of the TDC will be described. Next simulation results will be discussed and finally, conclusions are drawn.

2. Analogue TDC core blocks

To acquire a stable time measurement, the analogue front-end is based on a delay locked loop (DLL). An overview of the analogue front-end of the TDC is shown in Figure 1. The DLL continuously ensures that the delay line is synchronised to the period of the reference clock. This is done by the phase detector (PD), charge pump (CP) and loop filter (LF). The PD will measure the phase difference between the input reference clock and the delayed reference clock. According to this phase difference the charge pump is switched to change the control voltage, steering the total delay of the delay to be equal to the period of the reference clock. the reference clock used in this DLL is generated by a LC oscillator based PLL, which is proven to be Single event tolerant [8].

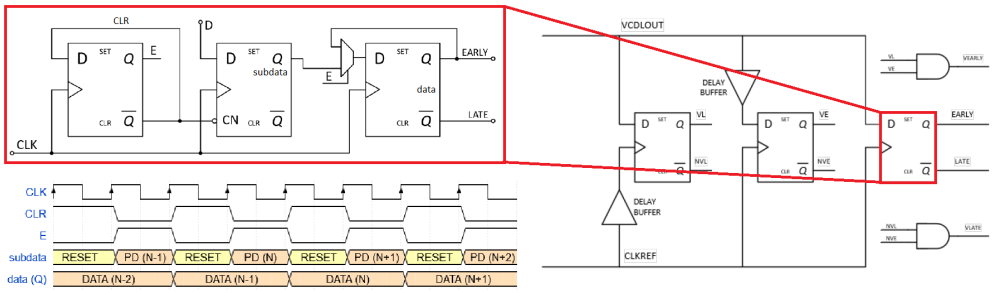

Figure 2: Novel Phase detector consisting of two blocks

2.1 Phase Detector

The phase detector proposed in this design has two important features: (1) the ability to generate four different output levels, depending on the time difference at the input and (2) an extremely low hysteresis. The first feature results in the ability to distinguish the phase between two signals in four levels: very-early, early, late, and very-late. The four levels are achieved by use of a 3-state controller with two delay elements (figure 2), the output of this controller represents the four different states. These states are used in the DLL to quickly recover from an out of lock state, which can happen in case of a SET close to the LF, where it will take much longer for a regular bang-bang PD to recover. An example of this fast recovery is shown in Figure 4. In this simulation, the different states of the PD can clearly be distinguished. In the beginning the loop is in a locked state. After the occurrence of an SET on the LF of the DLL, the control voltage drops to a low control voltage, which results in a small delay. The PD detects this very-small delay and enables a strong charge pump which results in a quick adjustment of the delay line. When eventually the delayed signal enters the narrow early-late range, the fast charge pump is switched-off and only the smaller charge pump will change the control voltage. By using this principle, the DLL is able to recover from a SET in less than 1 us and features a low in-lock limit cycle jitter.

The second novel contribution is the low hysteresis of the bang-bang detector. This addresses the problem of the sticky output of the phase detector, resulting in an unstable lock state and increasing limit-cycle jitter [6]. This issue is solved by using a modified phase detector shown in Figure 2 and placing a reset period before every phase detecting period. In this way, every phase detection starts from the same output state. A typical timing diagram of this phase detector is shown in Figure 2. By using this technique, the phase detection hysteresis is reduced but also the detection speed is reduced by half. This, however, results in a more stable lock state of the DLL, resulting in a decreased output jitter. As shown in Figure 3, simulations show that the benefits of having a lower hysteresis, outweigh the lower phase detection speed. The blue graph shows the timing jitter of the in-lock delay when using a regular phase detector. The red graph shows the delay when using the improved phase detector that is proposed in this paper. Comparing the two, the new phase detector results in a delay variation which is 40 times smaller compare to the conventional phase detector.

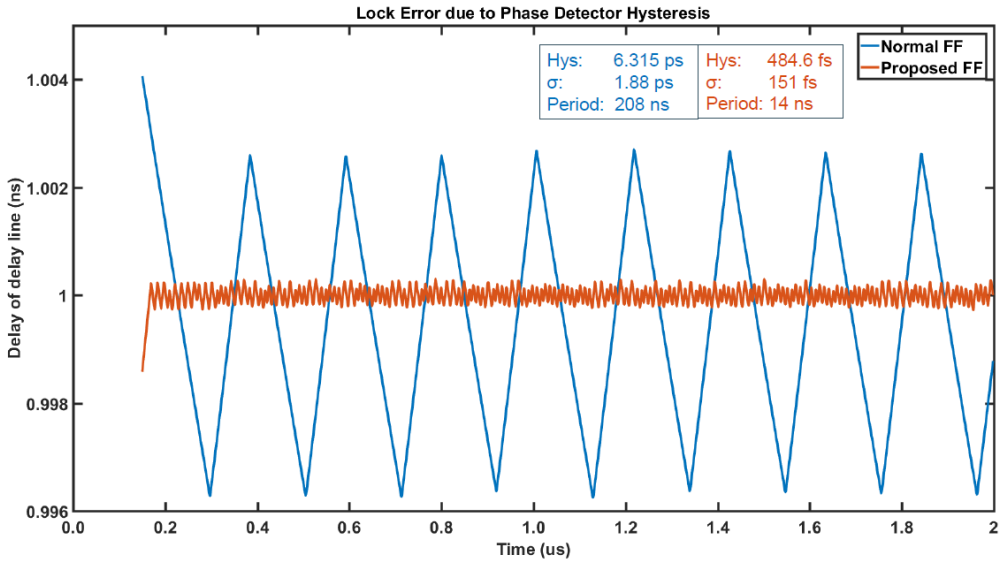

Figure 3: Hysteresis comparison, Blue: standard PD, Red: new PD

2.2 Delay Line

One of the goals of this TDC is the ability to make the TDC work in harsh environments. Therefore, it is important to foresee the ability to compensate for intrinsic process variability, while still aiming for a high resolution. The worst-case buffer delay in a 65 nm CMOS technology is around 40 ps. To realize an acceptable resolution every delay element is interpolated eight times, meeting the requirement of having $2^N th$ output levels. The delay of the buffer itself can be adjusted by means of an analog control voltage, which controls the current inside the (current-starved) delay-cell. Inside the DLL, the delay line is constantly adjusted to fit the period of the clock reference.

2.3 Charge Pump

As mentioned before, the DLL uses two charge pumps with different output currents. The CP with a small current is used when the delayed signal is either early or late. This means that the DLL is almost in the lock state and only small adjustments are required. If the delayed signal is very-early or very-late, the CP with a larger current is switched on, resulting in larger adjustments to bring the DLL faster to its lock state [7]. Both charge pumps are adjustable with a current DAC, this is useful to control the recovery speed of the DLL.

3. Conclusion

Several circuit techniques to improve radiation tolerance of CMOS Time-to-Digital converters, have been demonstrated, for both TID and SEUs. A multistate phase detector is used to quickly recover from an out of lock state due to an SEU. A novel bang-bang phase detector is presented with low hysteresis that results in an in lock error of 40 times lower compared to a regular bang-bang phase detector. Both improvements, enable an extremely fast recovery time below 1 us in combination with a small locked loop hysteresis of 500 fs.

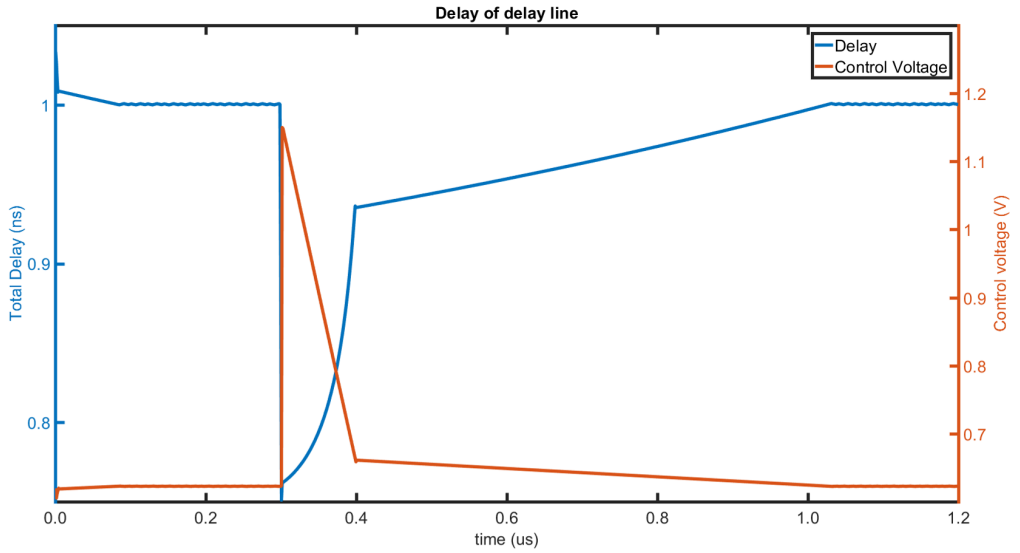

Figure 4: Signal Flow after SEU

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