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Electronics Developments for Phase-2 Upgrade of CMS Drift Tubes

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The Electronics for the Drift Tube Chambers (DT) of CMS will be significantly upgraded during the LHC Long Shutdown 3 (LS3). DTs are responsible for the tracking and triggering of muons in the central region of CMS. As a consequence of the higher L1A rate set by HL-LHC, the new CMS Trigger requirements will exceed the present capabilities of the DT on-detector electronics (so called MiniCrate, MiC). For this reason, having also in mind easier electronics maintainability and chamber aging mitigation arguments, DTs will replace all their MiCs during LS3. The phase-2 on detector electronics for DT will consist of a single type of board called OBDT (On Board electronics for Drift Tubes). A full description of the OBDT will be given along with the status of the prototype production and validation tests on the firmware.

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1. Introduction

Considerable enhancements are foreseen for the Drift Tubes (DT) subdetector during Phase-2 CMS upgrade. The new HL-LHC CMS Trigger/DAQ requirements exceed the present capabilities of the on detector electronics (MiniCrate, MiC) in terms of Level 1 trigger accept rate. As a consequence, together with MiC maintainability and chamber aging mitigation arguments, all MiC together with the associated back-end electronics will be replaced during Long Shutdown 3 (LS3). The partitioning of the electronics components between experimental cavern and service cavern will be re-optimized making use of the higher bandwidth optical link technologies now available at low cost. The main goal of the new electronics will be to allow better performing DT trigger algorithms, mitigating chamber aging effects and including new information made available in Phase-2 from the new tracker [1]. HLT resolution will be available at the L1 trigger and deadtime will be reduced to the minimum achievable by the present chamber. Another goal of the new on detector electronics is to get a more maintainable system. The present MiC is a complex system involving many different kinds of boards with several ASICs that date back to the 90s whose reliability after LS3 translates into a risk. A prototype of the new MiC, called OBDT, is going to be produced in 2018. Such prototype is built around a Microsemi PolarFire flash-based FPGA hosting 240 TDCs with the ns resolution. The timing and slow control distribution will be done by the GBT chipset while the data transfer will be performed directly through the fast serializers of the FPGA that are able to reach a transfer rate greater than 10Gbps. In view of the installation of a prototype of such electronics during the long shutdown of LHC, a demonstrator of the full trigger and readout chain was built at the CMS site in 2018. This paper will describe in Section 2 the evolution of DT electronics for Phase-2 upgrade including its demonstrator. A full description of the OBDT will be given in Section 3 along with the status of the prototype production and validation tests on the firmware. Finally a description of the next step in the upgrade process will be drawn in Section 4.

2. Phase 2 electronics upgrade for Drift Tubes

In the present architecture of the DT electronics, data are moved from the experimental cavern to the counting room via separate L1 Trigger and DAQ paths. Trigger primitives are generated in the dedicated electronics on the on-detector MiC and sent to the concentrator, called TwinMux, before reaching the track finder [2]. Due to the long distance between the two areas a copper to optical translation is performed by CuOF [3] relatively close to the detector. A similar path is followed by data that reach cDAQ after passing through the μROS [4] concentrator. The phase-2 on detector electronics for DT will consist of only a single type of board called OBDT (On Board electronics for Drift Tubes). The OBDT receives signal hits from each analog FE chip and assigns a digital timestamp. It hosts a multi-channel TDC implemented in a radiation hard FPGA and its associated services. The data are transferred out of the experimental cavern using high bandwidth optical link technology developed by CERN. Readout pipeline buffering and trigger primitive generation will be done in boards located outside the experimental cavern, profiting from the more relaxed environmental constraints.

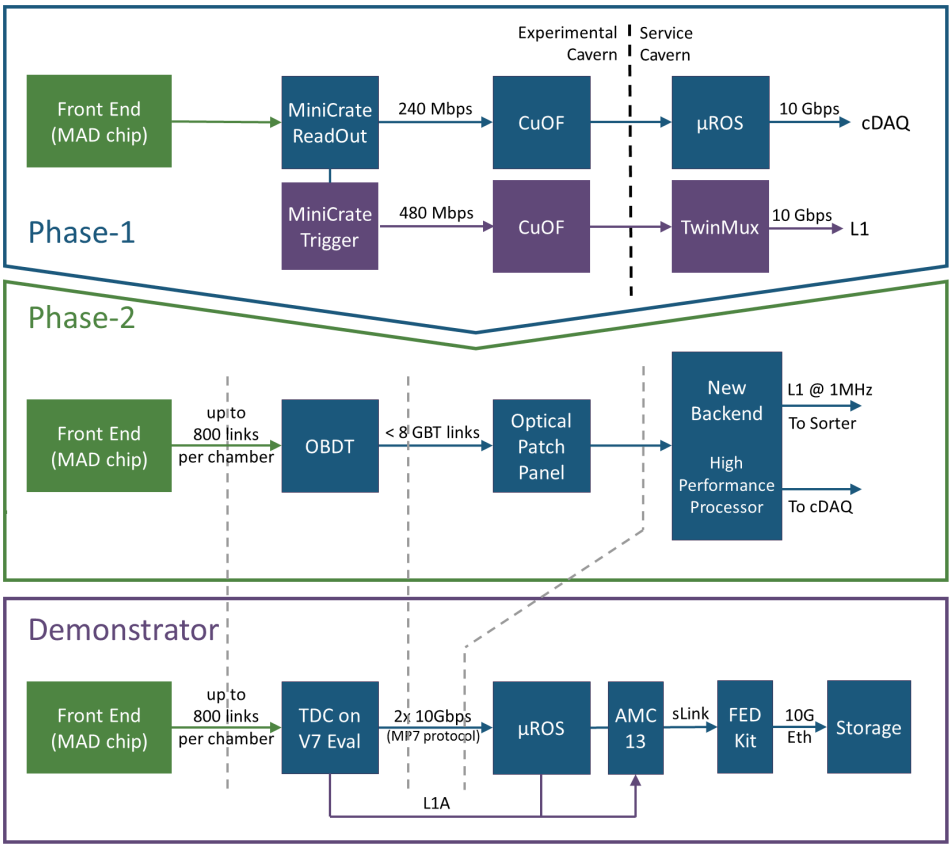


Figure 1: Block diagram of the actual Phase-1 electronics, its evolution for Phase-2 upgrade and the proposed demonstrator system.

2.1 The demonstrator

The demonstrator of the phase 2 electronics for Drift Tubes is designed for being a test stand for different hardware from the front-end to the back-end electronics. Its modularity make it easy to evolve at the same pace of the electronics towards LS3. It consists of a DT (Drift Tubes) chamber equipped with a full trigger and readout chain. As a first step the Phase 1 upgrade back-end electronics has been used for qualifying a demonstrator of the onboard Phase-2 electronics. A Virtex7 FPGA hosting 138 TDCs (1ns resolution) was used to timestamp the hits collected from the front-end analog discriminators. The hits are then moved through high-speed links (10Gbps) towards the back-end that is responsible for buffering the data and trigger generation. The triggered data are read out with the CMS standard acquisition chain until the data storage on disk. The next step in the evolution of the setup will be the substitution of the front-end FPGA with a prototype of the OBDT board.

3. On Board electronics for Drift Tubes

OBDT is a custom made board built around a Microsemi Polarfire Flash-based FPGA. It receives 240 LVDS pairs from the DT front-end comparators through eight flat cable connectors.

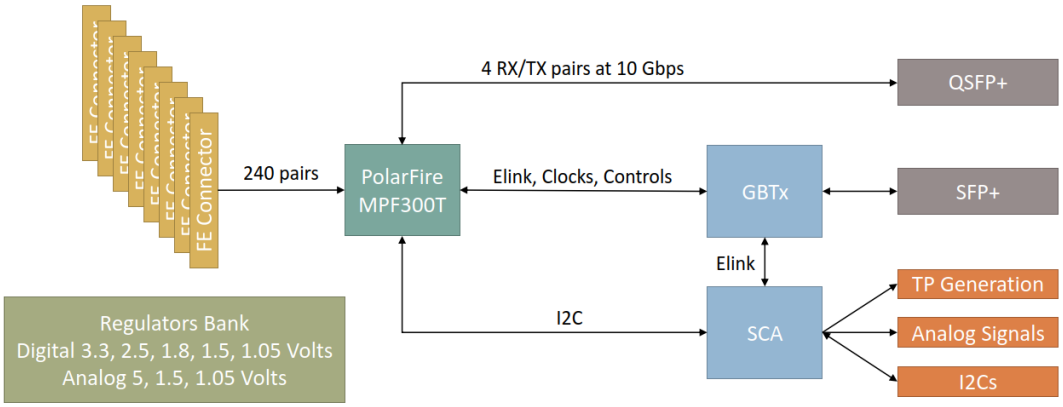
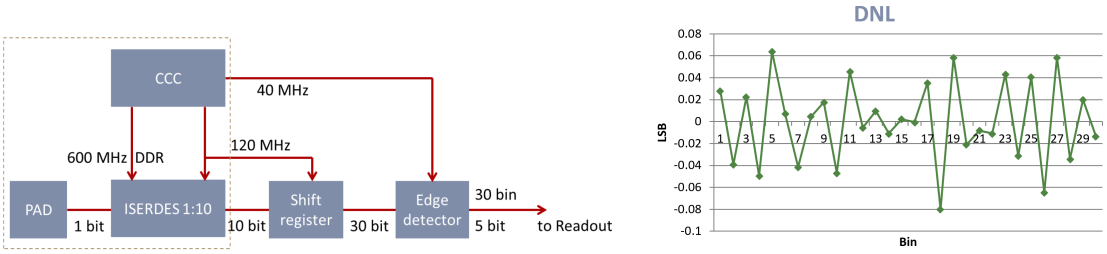


Figure 2: OBDT block diagram. The three main components are a Polarfire FPGA from Microsemi and the GBTx and SCA chips developed at CERN. The FPGA inputs are 240 LVDS lanes and for the output a QSFP+ transceiver is used. It can transfer data at up to 12 Gbps on each of the four lanes. The GBTx and SCA chip are used for slow control and time distribution. The connection to them is guaranteed by means of an SFP+ transceiver.

Four bidirectional high speed lanes (12 Gbps) are used for transmitting data to the back-end via a QSFP+ optical transceiver. Another transceiver (SFP+) will be dedicated for the GBTx, which will provide the recovered LHC clock as well as fast and slow control. The SCA will generate analog signals for the front-end, such as pulse and comparator thresholds, and also provide I2C communication. It will be also used for the reprogramming of the FPGA through JTAG port. A redundant path for slow control is foreseen: in case of failure of the optical link of the GBTx, the SCA and GBTx can be accessed from the FPGA through the Elink and I2C respectively. A flash memory is also adopted for guaranteeing the reprogramming of the FPGA through the QSFP+, in case of failure of the main slow control link. In this case the FPGA itself will load the new firmware on the flash and it will be configured at the next power-cycle of the board. OBDT is a 12 layer board with a stack-up defined in order to route the high speed signals on internal layers. A ground plane is used for shielding any possible noise such lanes can generate to the delicate front-end electronics. Stacked microvias are used to cross the ground plane without leaving any stub on the high speed traces. The layout has been extensively tested with the simulation tool SiWave from Ansys [5] for power and signal integrity. The geometry of the high speed vias has been carefully adjusted to avoid mismatch of impedance.

Although the board is not yet assembled due to delays in the production of the Polarfire FPGA, the firmware is already being developed targeting its evaluation board by Microsemi. At the input stage a Time to Digital Converter (TDC) is used for tagging the front-end pulses with a nanosecond resolution. The block diagram of the TDC is sketched in Figure 3(a). The input deserializer is used for sampling the incoming pulses at 1.2Gbps (600MHz in double data rate). A deserialization factor of 1:10 and afterwards a shift register decrease the clock frequency until obtaining a 30 bit word at the LHC clock frequency (40MHz). In such a way an edge detector can analyze the word and assign a TDC measurement according to the position of the rising edge of the pulse. Although 240 TDCs can be deployed on the OBDT board only 32 could be tested on the evaluation board

due to a limited number of general purpose inputs available. The linearity of the TDC has been measured using the code transition location method based on random (flat) input distribution [6]. A DNL well below 0.2 lsb has been achieved. Figure 3(b) shows the DNL distribution for each TDC bin.



(a) (b)

Figure 3: (a) Time to Digital Converter (TDC) block diagram. The Clock Conditioning Circuit provides the clock for the two deserialization stages of the TDC. The first is achieved by the embedded hardware deserializer of the FPGA, while the second is realized in logic. At the end an edge detector finds the rising edge of the input signal and it assigns a TDC measurement. (b) DNL of the TDC for each bin.

4. Conclusions

The first steps in building a prototype of the DT on-board electronics for Phase-2 upgrade have been shown along with a firmware development for a TDC. A linearity measurement shows that a multi-channel TDC with nanosecond resolution is achievable with a flash-based FPGA. The full qualification of the TDC will be completed as soon as the prototype OBDT is fully assembled. During LS2 (2019-2020) a DT sector will be equipped with the OBDT boards for demonstrating that the transmission of all the DT hits to the back-end is possible without the need for a dedicated trigger path. This simplifies the system and provides the Track Finders, within the L1 Trigger, access to the full data set for optimum performance.

References

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