A possible implementation of a detector specific extension of the FELIX firmware for the ITk Pixel sub-detector

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For the ATLAS Phase-II upgrade, a completely new all-silicon inner tracker is planned, which will be read out at higher bandwidth due to finer granularity and higher occupancy. At that point, the detector readout will be switched to the new ATLAS wide readout system focusing on the usage of the GBT protocol and introducing the FELIX concept. While the ITk Pixel sub-detector allows the usage of the GBT protocol on the downlink path, it needs a different uplink protocol due to certain constrains. This work shows how a detector specific extension of the FELIX firmware could look like and which blocks are needed for the ITk Pixel sub-detector.

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1. Introduction

In the course of the HL-LHC upgrade (2024-2026) [1], ATLAS will perform the Phase-II upgrade to handle the expected luminosities of up to $5 \cdot 10^{34} \, \text{cm}^{-2} \, \text{s}^{-1}$. During this upgrade the complete Inner Detector of ATLAS will be replaced by the new **I**nner **T**rac**k**er (ITk).

While the ITk Pixel sub-detector allows the usage of the GBT protocol [2] on the downlink path towards the detector, it needs a different uplink protocol (i.e. the AURORA protocol [3]) due to the lpGBT chip not being radiation hard enough to be placed where it would be needed and the high data rates (up to 4x 1.28 Gb/s per front-end) to be driven over several meters until conversion into optical signals.

The new ATLAS-wide readout cards called FELIX (FrontEnd LInk eXchange) [4] will be used for translation between the front-end links and a commercial networking environment, in which all further processing steps are located. To meet the specific requirements of the ITk detector, this FELIX card needs some front-end specific firmware extensions.

This work shows a possible implementation of such a firmware extension for the ITk Pixel sub-detector. It includes conversion of TTC (Trigger, Timing and Control) signals into commands for the front-end chips as well as support for trigger tags instead of Bunch Crossing ID and Trigger ID for event identification for the downlink path. On the uplink side, an AURORA decoder block will be used for deserialisation and descrambling. Also, decoders and monitoring blocks are needed for low-level error handling and busy propagation.

2. Structure of the FELIX Firmware

The current readout structure is based on detector specific electronics encapsulating the special needs of each subsystem. This requires each subsystem to have special trained experts to be able to
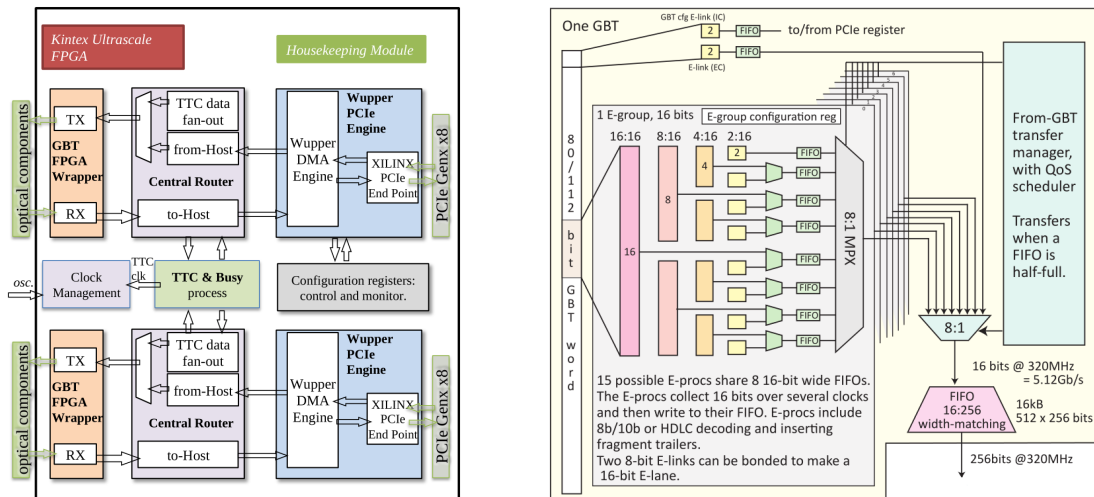
(a) Block diagram of the existing Phase I FELIX firmware, which still uses the GBTX protocol.

(b) Detailed view of the Central Router showing the uplink EProcs. The downlink path is in principle the same with direction of the data flow being inverted.

Figure 1: Structure of the FELIX Firmware. [5]

maintain their systems. In the course of the upgrade of the ATLAS detector, the readout will also be upgraded and unified. A result of this are the FELIX readout cards which will be used by all subsystems of ATLAS. As these will replace the detector specific readout electronics, some of its functionality needs to be adopted by FELIX.

Within the FELIX firmware, the Central Router is multiplexing and demultiplexing the data sent to and received from the detector. It uses so called E(lectrical)-Link Processors (EProcs) for stream handling. Thereby, each EProc handles the up- or downlink of a single GBT E-Link. (See Figure 1)

In case of the ITk detector, the FELIX card will be directly connected to detector electronics with only optical-to-electrical conversion in between and therefore needs to encode data being sent to the detector and decode the received data. This is the reason why specialized EProcs for the ITk detector are needed.
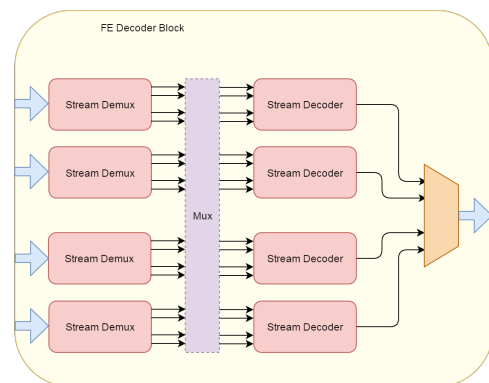
3. Downlink path towards the detector

On the downlink path, data from several sources needs to be interleaved and sent towards the detector. This includes trigger and global synchronization signals from the TTC system as well as data and commands from the readout software or continuous reconfiguration. The TTC frames can be sent at any time with no interference to read/write commands. This allows to reconfigure the detector without pausing triggers. The continuous reconfiguration is needed to mitigate single-event-upsets in configuration of the front-end ASICs which would lead to unwanted behavior of the pixel cells.

The TTC signals are encoded in the EProc while the readout software as well as the reconfiguration are using pre-encoded data streams. After sorting the different sources by priority, the frames are send to the detector. In the case when no source wants to send data, some IDLE frames are included. A block diagram can be found in Figure 2a.
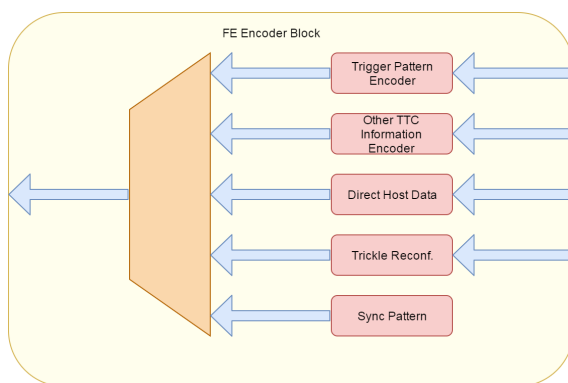
(a) Block diagram for the modified downlink EProc for ITk Pixel. It combines data from several sources to be send to the detector.

(b) Block diagram for the modified uplink EProc for ITk Pixel. It decodes four optical links.

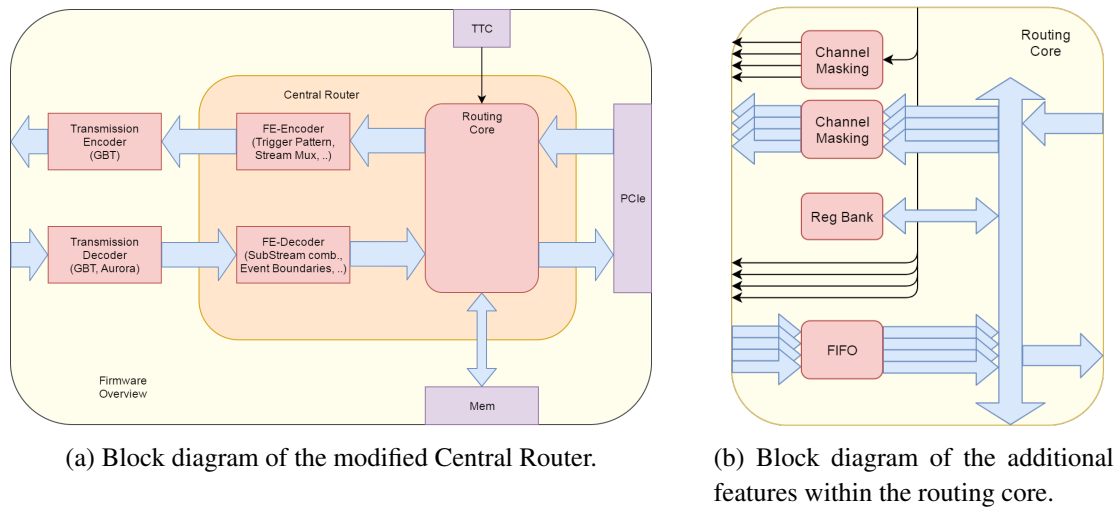Figure 2: Structure of the downlink and the uplink EProcs.

(a) Block diagram of the modified Central Router.

(b) Block diagram of the additional features within the routing core.

Figure 3: Updated structure of Phase I FELIX firmware

4. Uplink path from the detector

On the uplink path, the received AURORA stream must be deserialized, descrambled and the IDLE frames are dropped to reduce the occupied bandwidth. The incoming streams consist of several logical streams and need to be separated as these can come from different front-end chips. This is necessary for decoding status signals and masking of disabled links. An additional multiplexer for resorting the data streams may be needed as the cabling scheme within the detector is not fixed yet and data from a single front-end chip can be split up on up to four optical links.

After decoding, the filtered data frames are forwarded to the Routing Core and transmitted to the designated target. A block diagram can be found in Figure 2b.

5. Update on Phase I FELIX firmware

Besides the modified EProcs, also changes in the global firmware structure are needed. As the current configuration used for continuous reconfiguration must be stored somewhere and will not fit into the FPGA internal resources, some external memory is needed. A possible solution for this could be the usage of the host system memory. But this would require additional bandwidth on the PCIe interface. Another option would be to place external memory chips directly in the FELIX card, which are not there in the current version. This will increase the complexity of the card, but offers independent access so can also be used to capture raw data and help in debugging.

A second block of adaptations is required by the usage of trigger tags which are used instead of the Bunch Crossing ID (BCID) and the Level 1 ID (L1ID) used by the global trigger system of ATLAS. These tags need to be generated in a deterministic way and replaced later in the processing path. Thereby, several events can have the same tag[1] as the triggers can be grouped into a single trigger frame on the downlink. This complicates tag handling as grouping depends on internal status of the FELIX firmware.

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[1]The tags will get an additional extension in the FE chip so that the different events can still be identified.

Name	Slice LUTs (433200)	Slice Registers (866400)	Slice (108300)	LUT as Logic (433200)	LUT as Memory (174200)	LUT Flip Flop Pairs (433200)
i_RD53A_DL_EProc (RD53A_DL_EProc_4008)	66	105	35	66	0	105
i_fifoControler (fifoControler_4009)	0	17	4	0	0	13
i_merger (merger_4010)	5	20	9	5	0	22
i_serializer (serializer_4011)	14	20	10	14	0	22
i_syncEncoder (syncEncoder_4012)	19	21	12	19	0	25
i_trigEncoder (trigEncoder_4013)	24	20	16	24	0	38
i_ttcEncoder (ttcEncoder_4014)	5	7	3	5	0	9

Figure 4: Resource usage of the modified downlink EProc. There will be up to 48 downlink EProcs in the final firmware.

6. Results

Even with this paper describing work in progress, some first results have been achieved. A basic implementation of the downlink path was integrated into the FELIX firmware and tested successfully by configuring a front-end ASIC. While it has all the interfaces needed to meet the requirements, only the data path from the readout software is connected. Figure 4 shows the resource usage of the downlink EProc.

7. Conclusion

The new ITk detector will require several modifications to the firmware of the FELIX card. Whereas first parts are already implemented, more investigation and further input from other groups are needed for the main part of the modifications as other components of the readout chain (e.g. connection scheme within the detector) are not fixed yet.

A first draft version of the modified downlink EProc exists and the uplink part will be implemented in the near future. Both will be used to test and verify several assumptions.

Acknowledgments

References

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[3] Xilinx, Aurora 64B/66B Protocol Specification https://www.xilinx.com/support/documentation/ip_documentation/aurora_64b66b_protocol_spec_sp011.pdf

[4] The ATLAS Collaboration, ATLAS Trigger and Data Acquisition Phase-II Upgrade Technical Design Report, ATL-COM-DAQ-2017-185 CERN (2017), https://cds.cern.ch/record/2296879/

[5] ATLAS FELIX Group, FELIX Phase-1 Technical Specification and Implementation Final Design Review, CERN (2018), https://atlas-project-felix.web.cern.ch/atlas-project-felix/docs/FelixPhase1FDR.pdf