

## Remote Control Unit of the LHC Injector Complex Beam Loss Monitoring System

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**Eva Calvo\*, William Viganó and Christos Zamantzas**

*CERN*

*CH-1211, Geneva 23, Switzerland*

*E-mail: [eva.calvo.giraldo@cern.ch](mailto:eva.calvo.giraldo@cern.ch), [william.vigano@cern.ch](mailto:william.vigano@cern.ch),  
[christos.zamantzas@cern.ch](mailto:christos.zamantzas@cern.ch)*

The strategy for beam set-up and machine protection of the accelerators at the European Organization for Nuclear Research (CERN) relies strongly on their Beam Loss Monitoring (BLM) systems. The BLM system of the CERN PS complex (PS, PS Booster and Linac4) was recently renovated. The upgrade aimed to extend the dynamic range in order to accept more types of detectors and to obtain a highly reconfigurable system. The new acquisition system has shown very promising results, and development is now concentrated to provide advanced remote diagnostics, set-up and monitoring features. In this context, a new remotely controlled module is under design, which will continuously survey a set of status parameters (power consumption, temperature, etc.). Additionally, by controlling an embedded current source, it will allow the analogue circuit of each channel to be compensated for component tolerances, noise and ageing.

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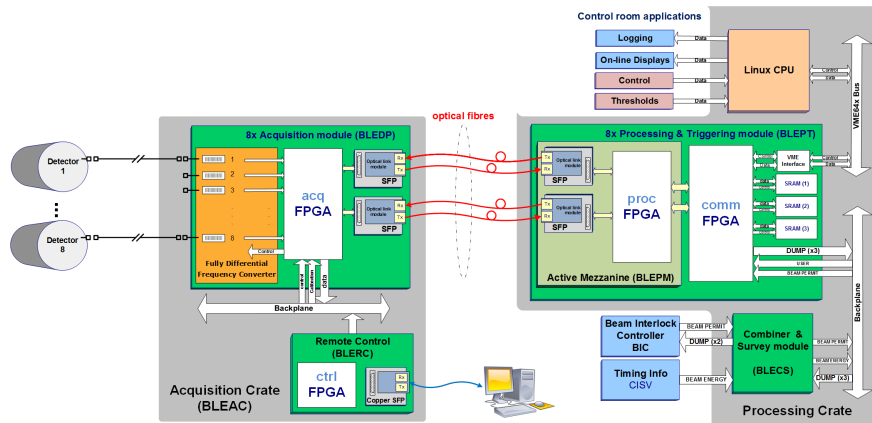
\*Speaker.

## 1. Introduction

The strategy for beam set-up and machine protection of the accelerators at the European Organization for Nuclear Research (CERN) relies strongly on the Beam Loss Monitoring (BLM) systems. The reliability of such a system directly affects the availability of the accelerator facility. Particular effort and attention has therefore been paid to include a complete set of features that allow the system to be constantly monitored, ensuring correct functioning and providing an alert if the observed parameters deviate from predefined levels. The present paper will describe the additional diagnostic and calibration features added to the injector complex BLM system through a new module, the BLERC.

### 1.1 System Architecture

The BLM system of the CERN PS complex (PS, PS Booster and Linac4) was recently upgraded [3]. The upgrade aimed to extend the dynamic range, in order to accept more types of detectors and to obtain a highly reconfigurable and reliable system. As can be seen in Fig.1, the architecture is split into two crates.



**Figure 1:** LHC injector complex BLM system architecture

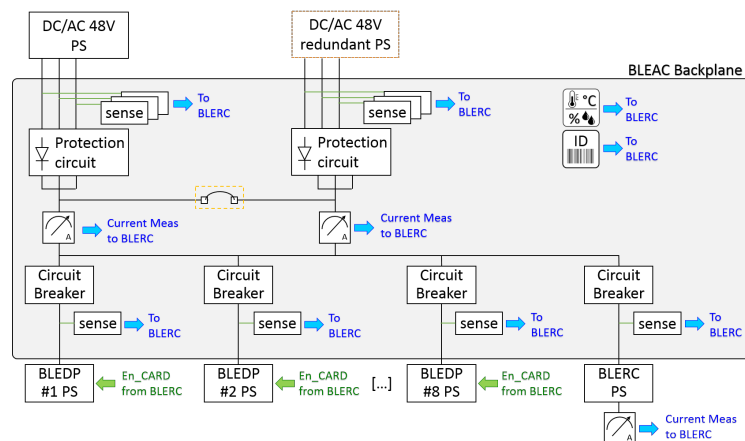
The front-end electronics (BLEAC) takes care of acquiring of up to 64 input channels. This crate is based on a custom designed backplane that provides connection for up to eight front-end acquisition modules (BLEDP cards) and the recently designed remote control unit (BLERC). The back-end processing crate is of a Wiener VME64x type. It hosts a Linux CPU, a timing receiver module, the combiner and survey module (BLECS) and up to eight processing and triggering modules (BLEPT).

Every BLEDP implements two different, parallel acquisition chains: a fully differential current to frequency converter (FDCF), able to cover a range from 10pA to 30mA, and the direct digitisation of the voltage drop in a reference resistor (DADC), which is used from 50uA to 200mA. An embedded FPGA acquires the results of one or the other method every 2us depending on the value obtained in the previous acquisition period [1, 2]. The measurement data, together with the channel number, method used and system status is grouped into TCP/IP frames and sent to the BLEPT processing module. The BLEPT maintains several parallel running sums in order to calculate the integrated losses for different time intervals (2us, 400us, 1ms and 1.2s) with the results

of each compared against a threshold every 2 $\mu$ s. The CPU publishes the processed data and status information for use by various control room applications. The BLECS control unit, located in the last slot of the processing crate, receives the two beam permit lines, which are then daisy chained through each BLEPT processing module. If any of these modules measures unacceptable losses the beam permit signal is removed, preventing future beam injections. The BLECS survey module also provides continuous supervision of the operation of the processing modules. If it discovers a disconnected module, a failure in the power supply or an error in the FPGA configuration it will also open the beam permit lines.

## 2. Acquisition crate diagnostics

The new BLERC control card constantly supervises the front-end acquisition crate, similarly to what the BLECS survey card does for the processing crate. In order to increase the system reliability, some redundancy has been implemented in the front-end crate and can now be exploited through the BLERC. As shown in Fig.2, a second power supply can be optionally mounted on the crate in parallel to the main supply. Two parallel shunt monitors constantly supervise the current provided by either or both supplies. Furthermore, the power supply outputs are routed through several lines and a feedback circuitry allows the BLERC card to sense the correct connection of each.



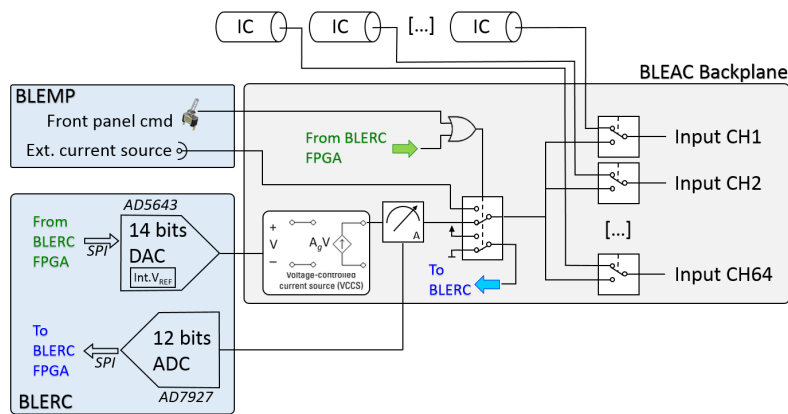
**Figure 2:** Remote diagnostics overview of the front-end acquisition crate

In addition, the crate backplane is equipped with a fail-safe circuit breaker, based on a high-voltage, power-limiting, hot-swap controller (TPS2491) at every front-end slot. These limit the inrush current and decouple the main power supplies from any eventual issue with the connected acquisition cards. The outputs of these controllers are fed back to the BLERC card. The BLERC card allows the remote enabling or disabling of every module independently, while continuously surveying the global current consumption.

All the gathered information together with the card identification number, the temperature and the humidity measurements of the crate and the BLERC card, are regularly published by the BLERC module, providing a complete overview of the health of the system.

### 3. System calibration

In order to guarantee correct and accurate measurements over many years, the BLERC card also performs the test and calibration of each acquisition channel. Fig.3 shows how this has been implemented. A 14-bit DAC (AD5643) controls a voltage controlled current source which has been embedded in the crate backplane. The generated current is measured by a shunt monitor whose output is digitised by a 12-bit SAR ADC (AD7927) on the BLERC. The current source has the ability to inject between 1mA and 40 mA with about 1% precision into any of the acquisition channels. This technique verifies the full scale functionality of the FDCF circuitry, compensates for offsets observed with the DADC method, optimizes the switching point between the two acquisition methods and monitors any possible degradation of the electronics through ageing.



**Figure 3:** Schematic of the embedded calibration system

Furthermore, the acquisition crate backplane contains a series of remotely controlled switches allowing each input channel to be connected either to the detectors (normal operation mode), the BLEAC embedded current source (for calibration or test) or to an external current source.

### 4. The BLERC firmware architecture

The BLERC firmware has been implemented on a Cyclone IV EP4CGX150CF23 FPGA. Its architecture is divided into three main functional blocks (Fig.4). The main logic block hosts the functionality responsible for gathering the crate status information from all the various sensor, such as the humidity sensors or the shunt monitors, as well as controlling and acquiring information on the embedded current source. Its main module, the Diagnostic Reader, contains as many interfaces as the number of devices it communicates with. It controls the different readout intervals, gathers the data of each interface and sorts them into a predefined data format. A scoreboard module monitors if every interface has updated its status since the last acquisition. Finally, the data is written into a dual-port memory which is mapped onto the memory space of a Soft-CPU.

The second block consists of a soft-core (SoC) and its peripherals. It is based on a NIOS II/f core, which works at 100MHz and is under the control of a  $\mu$ COS-II real-time operating system. This CPU is accompanied by a Triple Speed Ethernet (TSE) IP-core which implements the Gigabit

Ethernet MAC communication and includes the 1000BASE-X/SGMII Physical Coding Sublayer (PCS) logic. Three different on-chip memory modules have also been instantiated: one dual-port memory stores the diagnostic readout data; a second one stores the OS, program and data; and a third stores the memory descriptors used by the SGDMA cores. The embedded software implements a TCP/IP Ethernet server which periodically publishes the system status.

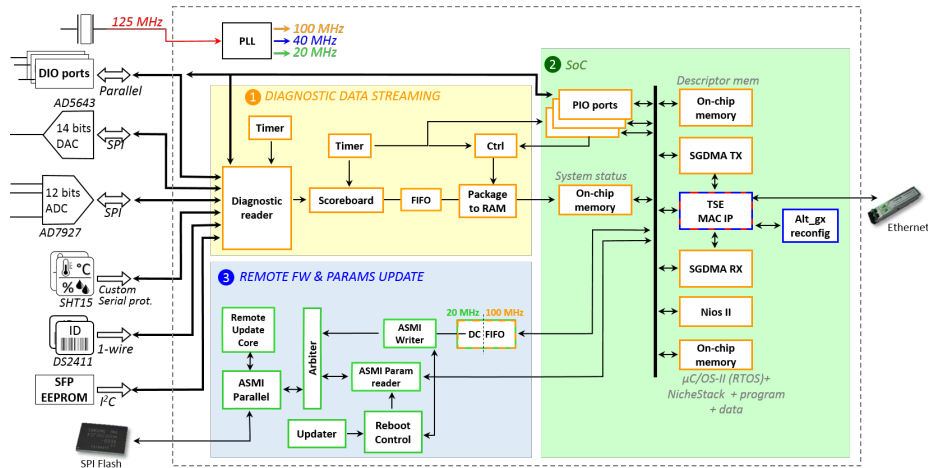


Figure 4: BLERC firmware architecture overview

The final functional block allows remote updates to the FPGA firmware, SoC program software, and default operational parameters. These are stored in SPI flash memory (EPCS128), arranged in such a way that two different configuration images are hosted: the factory and the application. The application configuration holds the last application firmware version, and is loaded after the factory configuration.

## 5. Conclusions

This paper presents the functionalities and architecture of a control module for enhanced diagnostics of the beam loss monitoring system used in the LHC injector complex. Several redundancy and reliability techniques have been implemented in the acquisition crate backplane and are now exploited by this module. In addition, the module provides the circuitry that allows the remote calibration and offset compensation of the front-end acquisition cards, as well as providing a means to test the full acquisition chain. This should result in a more dependable beam loss monitoring system.

## References

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