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A Low-Noise Charge-Sensitive Amplifier for Gain-less Charge Readout in High-Pressure Gas TPC

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We present a low-noise Charge-Sensitive Amplifier (CSA) manufactured in a standard 0.35 μm CMOS process. The CSA is part of an integrated sensor named *Topmetal-S*, an array of which forms a charge readout plane in a high-pressure gaseous TPC for 0νββ search. A single-ended folded cascode amplifier with a 73 dB open-loop gain and 340 MHz gain-bandwidth product forms the main amplification stage in this CSA. Measurements show that the conversion gain of the CSA with a 3 fF feedback capacitor is 163 mV/fC. With a 5 pF detector capacitance, the CSA achieved an equivalent noise charge of 28.7 e- using a digital trapezoidal pulse shaper.

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1. Introduction

The search for neutrinoless double-beta decay is one of the top priorities in the field of nuclear and particle physics. The experimental discovery of neutrinoless double-beta decay would confirm the Majorana nature of neutrinos and provide a measure of the absolute neutrino mass [1]. The predominant experimental signature of neutrinoless double-beta decay is a sharp peak at the decay Q-value $Q_{\beta\beta}$ in the total energy spectrum. Many techniques have been developed to search for such a signature with the utmost sensitivity. To date, the best sensitivity was demonstrated by KamLAND-Zen [2], which measures the energy spectrum through light output from ^{136}Xe loaded liquid scintillator. No positive results have been found and another order of magnitude improvement in sensitivity is expected to be necessary. Recently, high pressure gaseous, instrumented in a Time Projection Chamber (TPC), has been demonstrated to exhibit excellent intrinsic energy resolution at $Q_{\beta\beta}$ [3]. It is being explored by NEXT [4] and PandaX-III [5]. The NEXT experiment has chosen electroluminescence as the charge readout technology, which has both excellent energy resolution and beta tracking capabilities. The scalability, however, remains a challenge. The PandaX-III experiment in the first stage has chosen MicroMegas, but the additional fluctuation from electron-gas avalanche gain deteriorates the energy resolution.

The requirements for a potential discovery of neutrinoless double-beta decay point towards a tonne-scale experiment that is capable of observing a sharp peak at $Q_{\beta\beta}$ with 1% or better energy resolution and providing final state identification through mechanisms such as 2-β tracking and decay daughter identification. We are developing a direct charge sensor called *Topmetal-S,* which has one charge collection electrode on each sensor and is designed to form a large plane by tiling, is being developed to read out charge in a high-pressure gas TPC without gas-electron avalanche. This scheme eliminates the conventional avalanche fluctuations but demands exceedingly low noise on the Charge Sensitive Amplifier (CSA) to achieve sufficient energy resolution by charge measurement alone. The requirement of the Equivent Noise Charge (ENC) is less than 30 e^- [5]. The fine grained pixel tile at the same time provides final state identification through imaging the charge tracks in the TPC.

This paper shows the detailed design, simulation results and preliminary test results of the low-noise CSA built for a direct charge sensor for neutrinoless double-beta decay.

2. Internal structure of *Topmetal-S*

The internal structure of *Topmetal-S* is shown in Figure 1. Drifting electrons are collected by a Charge Collection Electrode (CCE) and then fed into the CSA. The charge signal is converted to voltage signal by the CSA and then split into two output channels. One channel transmits the analog signal off the chip through a unity-gain buffer. The signal in the other channel is digitized by a 16 bit Σ-Δ Analog-to-Digital Convertor (ADC) and then the digital code is transmitted through a Low Voltage Differential Signal (LVDS) interface. An exposed hexagonal metal node of 1 mm diameter is used as the CCE on the topmost layer. Its capacitance with respect to ground is around 5 pF. Charge collected by the CCE is DC coupled into the CSA. A guard ring surrounds the CCE. The parasitic capacitance between the guard ring and the CCE is about 1.186 fF, as extracted from the layout using the calibre pex tool. The guard ring serves two functions. On the one hand, a voltage pulse can be applied on the guard ring to inject test charge into the CSA for calibration. On the other hand, the electric field generated by biasing the guard ring helps to focus incoming charge onto the CCE.

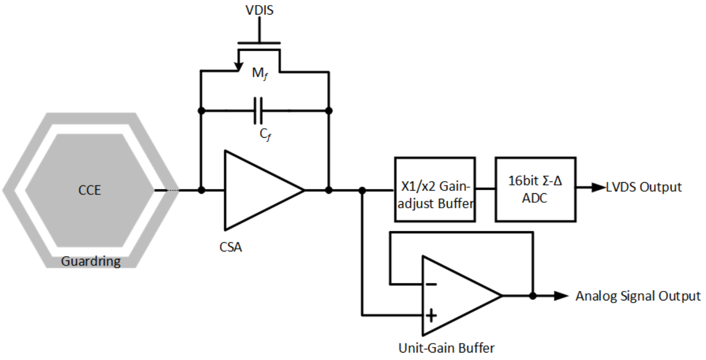

Figure 1: diagram of readout circuit in *Topmetal-S*

3. Charge Sensitive Amplifier

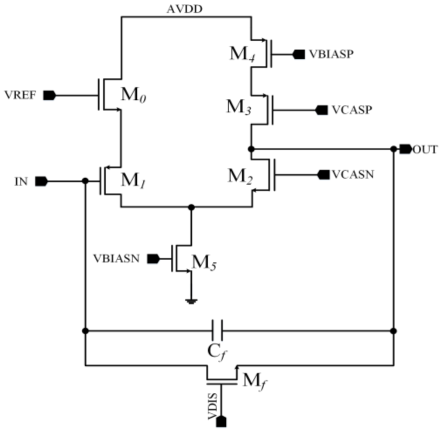

Figure 2: schematic of the charge sensitive amplifier.

Table 1: device dimensions

Name	W/L(μm/um)	Mf
M_0	20/1	200
M_1	10/0.35	76
M_2	6/1	12
M_3	10/0.35	1
M_4	2/10	1
M_5	10/12	50
M_f	1/5	1

The CSA structure is shown in Figure 2. The CSA is composed of an inverting amplifier and a small feedback capacitor (C_f), whose capacitance is well-controlled to be about 3 fF, as extracted from the layout using the calibre pex tool. The C_f is generated from the parasitic capacitance between metal 1 and metal 2. In order to reduce its variation, the shielding metals (metal 1, metal 2 and metal 3) are routed around the C_f to separate it from other routings and devices. The charge (Q) collected on the charge collection electrode is nearly fully integrated into C_f, hence the output signal amplitude (V_O) is approximately equal to Q/C_f, and the charge conversion gain A_Q=V_O/Q=1/C_f is determined by C_f. A regulated single-end folded cascode amplifier is implemented in this CSA. The dimensions of each transistor are shown in Table 1. The total width of each transistor is W * Multiplier factor (Mf). A p-type transistor is chosen as the input device because of its lower flicker noise contribution compared to an n-type transistor [6]. Meanwhile, the input transistor is optimized for a 1 mm sized CCE that has a ~5 pF capacitance to minimize the ENC [7]. All biases are independently tunable through Digital-to-Analog Converters (DACs) connected to them via low-pass filters. The operating point of 1 V, which is a normal reference point, could be tuned by adjusting the gate voltage of the n-type transistor added above the input p-type transistor. A reset transistor parallel to C_f continuously discharges C_f and restores the baseline. The RC constant could be extended into several milliseconds by controlling the gate voltage of the reset transistor. Lightly doped deep N-well surrounds each transistor to reduce the interference from the substrate.

4. Simulation Results

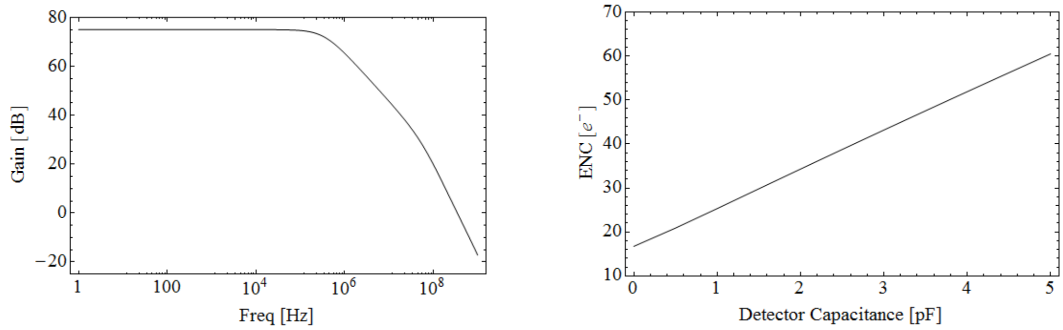

Figure 3: open-loop gain vs. frequency of the amplifier (left) and impact of the detector capacitance variation on the ENC (right).

Post-layout simulations show that the total current consumption of the CSA is about 2 mA and the rise time (20% ~ 80%) is less than 440 ns. The open-loop gain of the CMOS amplifier is about 73 dB and the gain-bandwidth production is around 340 MHz (left panel in Figure 3). The ENC is defined by the ratio between the rms noise (Vn,rms) at the output node and the signal amplitude (Vs,e-), normalized to electron charge: ENC = Vn,rms / Vs,e-. In the post-layout simulations without pulse shaper, the ENC is plotted as a function of the detector capacitance in the right panel of Figure 3. The ENC is estimated to be 16.7 e- + 8.8 e-/pF.

5. Preliminary Measurement Results

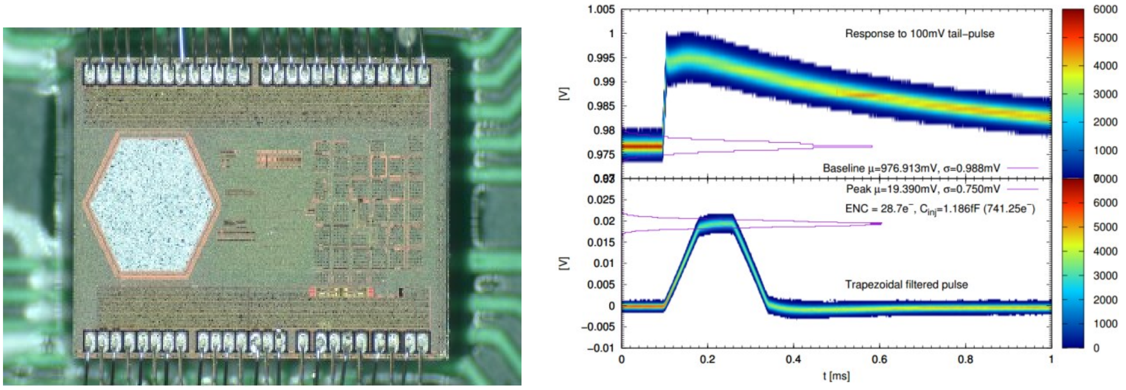

Figure 4: photography of *Topmetal-S* (left) and preliminary measurement results of the CSA (right)

The CSA, as part of the *Topmetal-S* sensor, was manufactured in a standard 0.35 μm CMOS process. The CSA occupies a 230 μm × 170 μm area. The entire *Topmetal-S* sensor has a dimension of 2 mm × 3 mm, shown in the left of Figure 4. For CSA testing, test pulses of 100 mV (ΔV) are injected through the C_{inj}. We record the analog signals transmitted through the analog buffer. Measurements show the mean output amplitude (V) is about 19.39 mV. Hence, the charge conversion gain of 163 mV/fC is calculated by $V/(C_{inj} * \Delta V/q)$, where q is 1.6 ∗

$10^{-19}C$. The C_{inj} and C_f has not yet been calibrated. The on-chip analog buffer is a unity-gain buffer. The equivalent noise charge of the CSA after an off-chip digital trapezoidal pulse shaper is 28.7 e^- rms at an optimum shaping time of about 180 µs. The precise operating point of the CSA during measurement is set by tuning the 6 bias voltages (Figure. 2) via built-in DACs. The goal of the tuning optimization was to achieve a stable operation while minimizing the ENC. We acknowledge that the ideal open loop gain was not achieved due to stability issues. The overall charge conversion gain achieved during measurement was lowered due to this. However, the target ENC was still achieved albeit this deficiency. An absolute charge conversion gain measurement using true electron injection from outside of the chip is on going.

6. Conclusions

A low-noise charge-sensitive amplifier for gain-less charge readout in high-pressure TPC is designed and manufactured in a standard 0.35 µm CMOS process. The preliminary measurement results show the CSA feactures an equivalent noise charge of 28.7 e^- after an off-chip digital trapezoidal pulse shaper, which satisfies the requirements for the readout of a high-pressure gas TPC for 0νββ

7. Acknowledgments

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