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The Readout and Data Transmission of a Monolithic Active Pixel Sensor prototype for the CEPC Vertex Detector

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We present the readout and data transmission of a MAPS prototype MIC4 for the R&D of the CEPC vertex detector. A new data-driven readout architecture is implemented to achieve high spatial resolution, fast readout, and low power consumption. MIC4 contains a matrix of 128 rows by 64 columns with a pixel pitch of 25 μm. By a periphery priority encoder circuit and a data readout and framing circuit, MIC4 readouts data real time without on-chip memory. An 8B10B encoder, a 10:1 serializer, and an LVDS driver are implemented to transmit serially the data at 1.2 Gbps.

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1. Introduction

The discovery of Higgs boson at approximately 125 GeV at the LHC [1,2] marks the beginning of a new era in particle physics. The Circular Electron Positron Collider (CEPC), operating at the center-of-mass energy of $\sqrt{S}$ ~ 240 GeV, has been proposed as a Higgs factory [3], which provides a good opportunity to investigate the Higgs boson. CEPC may also run at Z-pole to provide high statistics. In the future, CEPC will probably upgrade to higher energy (70–100 TeV) and become a super pp collider (SPPC)[3]. The luminosity of CEPC machine is expected to reach unprecedented 3×10^{34} $cm^{-2}s^{-1}$. The vertex detector which plays a critical role in heavy-flavor tagging, needs to be designed and optimized for this environment. The vertex detector of the CEPC requires radiation tolerance, low material budget, high spatial resolution, fast readout, and low power consumption. As the closest detector to the interaction point, the spatial resolution of the vertex detector needs better than 3 μm to improve the efficiency of heavy quarks and τ leptons tagging, and the material budget needs below 0.15% X0 per layer. According to the preliminary estimation, the detector occupancy does not exceed 1% and the radiation tolerance should be ~1 MRad/year and 2×10^{12} 1 MeV n_{eq}/cm^2/year for Total Ionizing Dose (TID) and Non-Ionizing Energy Loss (NIEL), respectively. The power consumption and the readout time of the sensor should be less than 50 mW/cm^2 and 20 μs, respectively. The Monolithic Active Pixel Sensor (MAPS) that had already demonstrated its excellent performance in several High Energy Physics experiments [4, 5] is the most promising candidate technology to satisfy all those requirements. We have studied two state-of-the-art MAPS sensors, ULTIMATE [4] and ALPIDE[5]. ULTIMATE is designed for the STAR Heavy Flavor Tracker (HFT) upgrade which uses the traditional rolling-shutter readout architecture. This architecture reads out all the data of the matrix without any data loss. However, when the occupancy is low, the readout efficiency is very low. ALPIDE is developed for the ALICE Inner Tracking System (ITS) which uses a data-driven readout architecture. Compared to the rolling-shutter scheme, both the integration time and the power consumption are improved using the data-driven scheme. However, the spatial resolution of ALPIDE cannot meet the requirements of the CEPC vertex detector.

In this paper, a MAPS prototype, MIC4 (MAPS In CCNU 4), for the R&D of the CEPC vertex detector is presented, with emphasis on the readout and data transmission. A new data-driven readout architecture is proposed which combines the priority Address Encoder and Reset Decoder (AERD) scheme [6] with the projection scheme to achieve high granularity together with fast readout speed. The remainder of the paper is organized as follows: Section 2 describes the design of MIC4. The test setup and preliminary test results of MIC4 are presented in section 3. Section 4 summarizes the paper.

2. Design of MIC4

MIC4 is designed with TowerJazz 180-nm CMOS Image Sensor process. The block diagram, layout and a picture of MIC4 are shown in Figure 1. It contains 128 rows and 64 columns with a small pixel pitch of 25 μm. Each pixel contains a sensing diode, an amplifier, a discriminator, and a hit storage register connected to a sparsified readout circuitry. The peaking time and duration time of the front-end is 1 μs and 3 μs, respectively. The Equivalent Noise Charge

(ENC) is about 10 e-, and the power consumption is 110 nW/pixel.

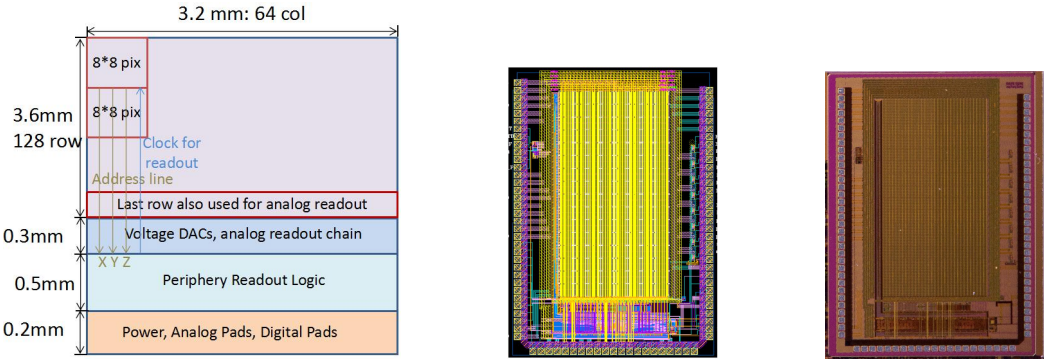

Figure 1: The block diagram, layout and a picture of MIC4.

2.1 Pixel array readout

In order to improve the spatial resolution, we combine the projection scheme and the AERD scheme in the pixel array readout of MIC4 to reduce the pixel area. Compared with the AERD scheme, the projection scheme has no encoding logic in pixels, so the pixels are smaller. The matrix of MIC4 is divided into groups called Super Pixel, each Supper Pixel has 8 × 8 pixels, as shown in Figure 2. Thus MIC4 has 8 Super Pixel columns, each column containing 16 Super Pixels. Each Super Pixel uses the two-dimension projection (X and Y directions) to identify the address of each hit pixel. The two-dimension projections of the 16 Super Pixels in one column are connected together, which are labeled as ADDRX<0:7> and ADDRY<0:7>. An OR gate chain is used to implement the data suppression in each Supper Pixel. Considering the effect of the propagation delay of the OR gate chain on the readout speed, the length of the chain should not be too long. So the addresses of the 16 Super Pixels in one column is readout through the same AERD architecture of the ALPIDE chip, which is labeled as ADDR<0:3>. The arbitration tree structure of the AERD scheme can reduce the length of lines, thereby decreasing their capacitive loads, and has the characteristics of low dynamic power consumption and high readout speed.

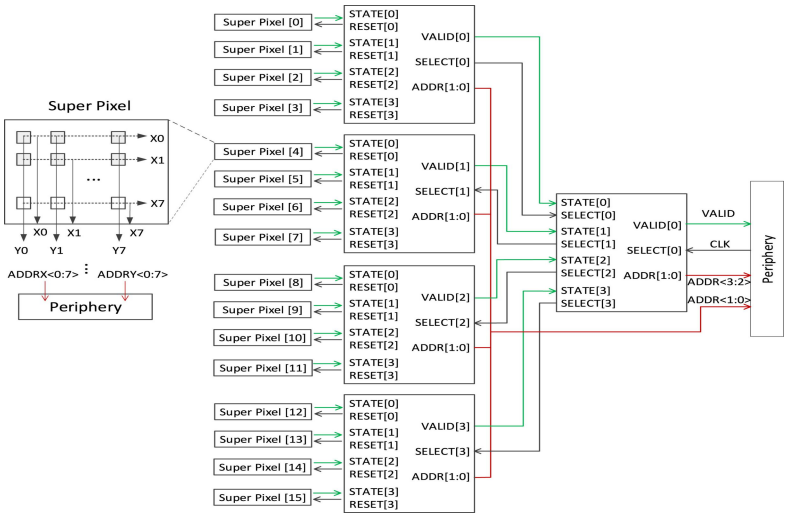

Figure 2: The pixel array readout scheme of MIC4.

2.2 Periphery readout and data transmission

A block diagram of the periphery readout and data transmission of MIC4 is shown in Figure 3.

In the periphery of MIC4, a periphery AERD circuit called PAERD has been implemented to identify the addresses of 8 Super Pixel columns. PAERD receives 20-bit address from each Super Pixel column and adds additional 3-bit to form a 23-bit pixel address. A data readout and framing circuit called DROF interacts with PAERD to read the hit pixel address at the rate of 40 MHz/hit. DROF is also responsible for forming data frames. The frame of MIC4 has 384 bits, including an 8-bit comma word K28.5 as the frame header and an 8-bit frame trailer to identify the number of valid data in the payload. No large memory is used to store frames and only a small FIFO is used to convert the data bit width. The DROF writes the 23-bit-width hit pixel address to the FIFO at the rate of 40 MHz in real time and inserts the frame header and the frame trailer according to the frame definition. MIC4 has two means of data transmission, a 120 MHz parallel data port that directly reads out the 8-bit data from the FIFO and a 1.2 Gbps serial transmission port that is implemented by an 8B10B encoder, a 10:1 serializer, and an LVDS driver in the periphery.

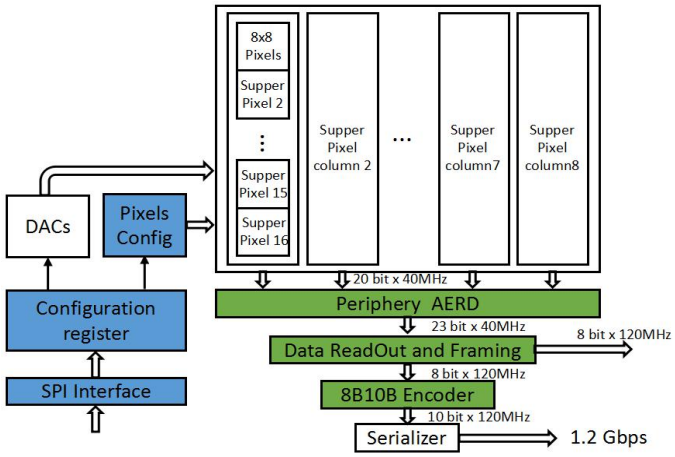

Figure 3: The periphery readout and data transmission scheme of MIC4.

3. Tests of MIC4 readout and data transmission

MIC4 is being evaluated. The test system consists of a test board, a Kintex-7 FPGA, an oscilloscope, and control software on PC, as shown in Figure 4. The FPGA implements an SPI master to configure MIC4, a deserializer to convert the serial data into the parallel data, an 8B10B decoder to recover the original data, and a 10Gbps TCP/IP module to receive test commands from the control software and transmit the addresses of hit pixels to the PC.

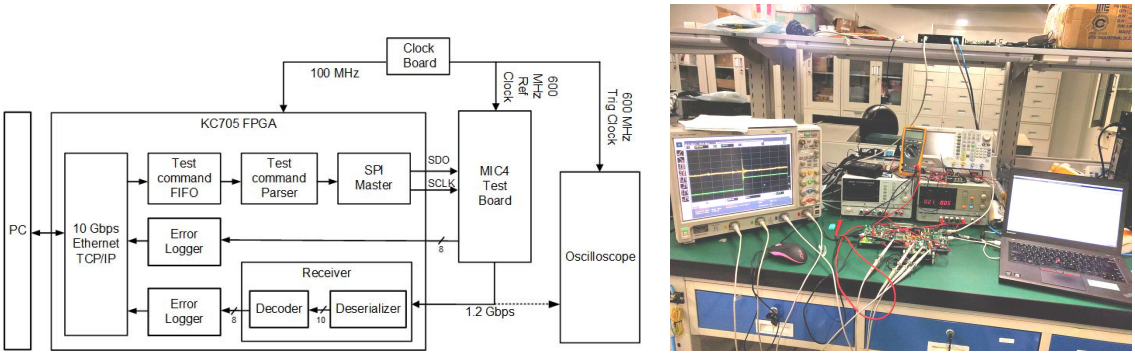

Figure 4: The block diagram of the test setup and a picture of the test setup.

In the preliminary tests, the output data frame structure of MIC4 and the address data of hit pixels were observed by oscilloscope when charge was injected into pixels, as shown in

Figure 5 (a). We also tested the parallel data transmission of MIC4 through FPGA. By opening some pixels and masking the remaining pixels to observe whether the readout pixel addresses are expected. No error was observed in the test. Figure 5 (b) shows an output eye diagram of MIC4 at 1.2 Gbps.

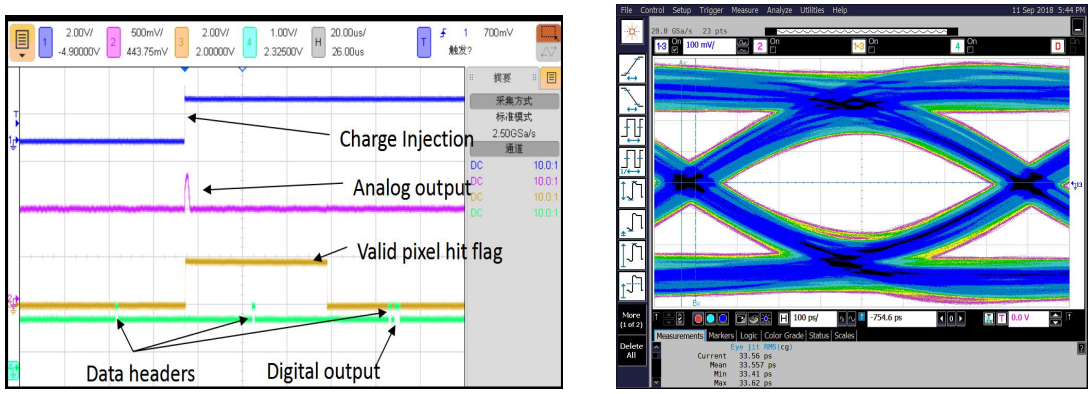

Figure 5: (a) The readout test through Oscilloscope. (b) The output eye diagram of MIC4 at 1.2Gbps.

4. Conclusion

For the R&D of the CEPC vertex detector, we have developed a MAPS prototype, MIC4, in TowerJazz 180-nm CMOS Image Sensor process. The design and preliminary test results of the readout and data transmission of MIC4 are presented. MIC4 implemented a new data-driven pixel array readout architecture based on AERD and projection. In the periphery, through a periphery AERD circuit, a data readout and framing circuit, MIC4 outputs 8-bit parallel data real time without on-chip memory. MIC4 can also output 1.2 Gbps serial data by an 8B10B encoder, a 10:1 serializer, and an LVDS driver in the periphery.

Acknowledgments

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