PROCEEDINGS OF SCIENCE

ALICE Trigger System for LHC Run 3

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The ALICE Central Trigger System (CTS) will be upgraded for LHC Run 3 with a completely new hardware and a new Trigger and Timing System (TTS) based on a Passive Optical Network (PON) system. A new universal trigger board was designed that can function as a Central Trigger Processor (CTP) or as a Local Trigger Unit (LTU). It is based on the Xilinx Kintex Ultrascale FPGA and upgraded TTC-PON. The new trigger system and the results of the tests and verification of the first 23 boards, produced at the beginning of 2018, will be presented.

Topical Workshop on Electronics for Particle Physics (TWEPP2018)
17-21 September 2018
Antwerp, Belgium

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PoS(TWEPP2018)119

1. Introduction

In LHC Run 3 the interaction rates in ALICE at LHC point 2 will increase from 8 kHz to 50 kHz for Pb-Pb, and from 100 kHz to 200 kHz for pp and p-A. An additional factor two safety margin is applied in the system design, where possible. The aim of the ALICE trigger system is to select essentially all of these interactions [1].

1.1 General description of the ALICE Central Trigger Processor for LHC Run 3

The new ALICE Central Trigger Processor (CTP) will be based on 3 possible trigger latencies (LM at 650 ns, L0 at 900 ns and L1 at 6.5 μs) with two modes of operation, a continuous mode and a triggered mode [1]. Its main function is to flag the time for each interaction, rather than to aim for selectivity, since in the new "triggerless" design event selection is done by a very large processor farm filtering events in real time. The layout of the trigger system, showing the connections between the main components, is shown in Fig. 1. Each detector will only use one trigger latency (except for the Charge Particle Veto (CPV) and Photon Spectrometer (PHOS) detectors, which use the old readout system). The main ALICE trigger will be sensitive to the LM trigger (all interactions). Other specialized triggers will arrive at the L0 or L1 trigger latencies, leading to refinements in the trigger selectivity for detectors that use these later latencies. Detectors running in continuous mode will receive regular "Heartbeat" (HB) triggers for synchronization. The trigger system must also cope with detectors that still have dead-time during the readout. The main interface between the Local Trigger Unit (LTU) and the Common Readout Unit (CRU) will be TTC-PON (Trigger Timing and Control via Passive Optical Network) [2], but the Inner Tracking System (ITS) and Muon Forward Tracker (MFT) detectors will also receive triggers directly at their Front End Electronics (FEE) via GBT (GigaBit Transceiver)[3] (in parallel to the CRU via TTC-PON) due to trigger latency constraints. The interface between the CTP and the LTU is also based on TTC-PON. The LTU will collect all CRU status messages, (e.g. Ready and FE link problems) from the detectors and forward these to the CTP, where an overall CRU status map will be built.

The CTP/LTU board is a universal trigger board, which can function as a CTP or as a LTU. It has 6U VME format, but it uses the VME backplane only to take power from it. The main component is a Xilinx Kintex Ultrascale FPGA. The logic for several interfaces is implemented: upgraded TTC-PON, GBT, IPbus [4], I2C, SPI and also the original TTC [5]. The board is equipped with 2 DDR4 memories (each 1 GB) and it can be equipped with a maximum of 20 SFP+ modules. A main SFP+ cage can accommodate 12 SFP+ modules and an additional 7 SFP+ modules can be connected by using a commercial FMC card FM S-18. A single SFP+ cage is always dedicated to the IPbus and provides control for CTP/LTU board. For high quality clock distribution, the Si5345-D PLL has been chosen. There are 2 such PLLs. One provides a free-running clock for the FPGA while the second PLL can be locked to a clock reconstructed from the ONU or a clock from a front panel. A selection of input clock for the second PLL is done via an I2C interface. There are 12 different voltages on the board, so a complex power system is controlled by a UCD90120A power sequencer from Texas Instruments and is monitored via a Power Management (PM) bus. A front panel is offering several types of connectors and LEDs are used for indication of different functionalities. One LED is also connected to a global AND of all Power Good statuses, so a user can immediately see if there is a problem with a power on the board.

The CTP board has to receive up to 34 trigger inputs in LVDS format, so an FMC CTP card has been developed for this purpose. It has 70 LVDS channels which can be configured as input or output in groups of 4. The Samtec SEAF type connector has been chosen for the input cable as its size fits the FMC card. A corresponding SEAC connector is used on a cable which brings trigger inputs from a patch panel to the CTP board. A standard SEAC cable has second end customized with the differential LEMO connectors.

A standalone CTP/LTU board can be inserted into a special ELMA box which was developed. A standard ELMA box with a custom front and back panel is equipped with 2 internal AC-DC power supplies, 2 fans for cooling, a power switch and a fuse. The main use of the ELMA box will be in a detector lab, as it does away with the need for a VME crate.

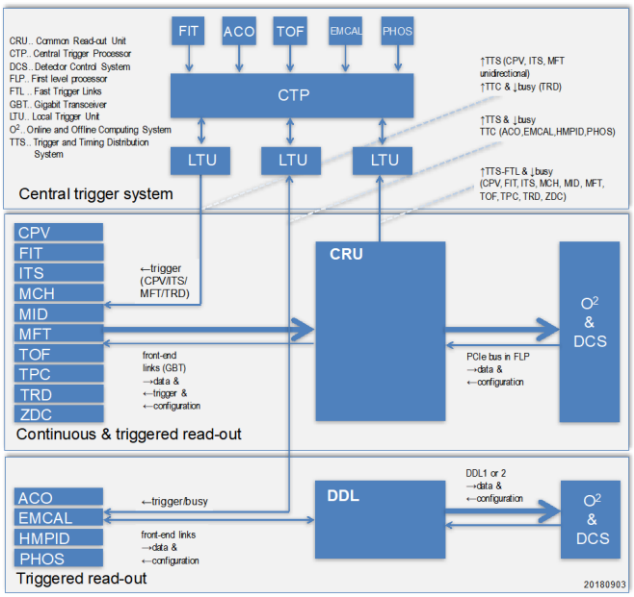

Figure 1. Block diagram showing layout of the ALICE trigger system, and its connections with the CRU.

2 Test results for 1-st production batch

In the first production phase, 6 VME boards and 17 ELMA boxes were produced. Two types of firmware and software have been developed for testing. The first type of firmware, called "IBERT+", is dedicated for the test of high-speed links (20 SFP+ modules) and is based on the Xilinx IBERT design, extended using a GT debugger with associated VIVADO TCL script for BER estimation using a data sample of 10^9. The Xilinx procedure involves a study of the eye diagram and gives us a very low BER, $<10^{-20}$, by extrapolation. A direct measurement over a 36 hour period using 9.6 Gbit s^{-1} data rate with PRBS 31 gives us $<10^{-16}$. All the boards were tested. Two boards were found to have faulty channels giving a higher BER. The rest were satisfactory.

2.1 TTC-PON temperature measurements for ALICE

The second type of firmware and software are used to test the functionality of all components connected to the Xilinx Kintex Ultrascale FPGA (upgraded TTC-PON, GBT, IPbus, I2C, SPI, the

original TTC and all components on the front panel). Each board has its own log file from the test.

A cascaded TTC-PON system, similar to the ALICE trigger system for LHC Run 3, has been built and has been used to verify full chain functionality. Two types of chain are used in the measurements: one is CTP-LTU-VLDB and the other is CTP-LTU-CRU-VLDB, as shown in Figure 2. The first type of chain has been used for tests using a climatic chamber, where clock jitter and clock phase stability have been measured at different temperatures. This measurement also includes a test of the reset procedure, where we have simulated different conditions after power-up or after the reset of the full chain. As an example, the results for one of these measurements are shown in Figure 3 for one temperature, showing values with and without resets. A blue line represents a clock skew without resets and a brown line the clock skew with resets. The wider range of clock skew with resets is mainly due to specific functionality in the high-speed transceiver of Xilinx Ultrascale FPGA. The inclusion of the CRU in the chain (not shown) makes the jitter deteriorate by 4 ps. The most stringent requirement on jitter is from the time-of-flight (TOF) system, which requires jitter to be under about 12 ps, and the system satisfies this requirement.

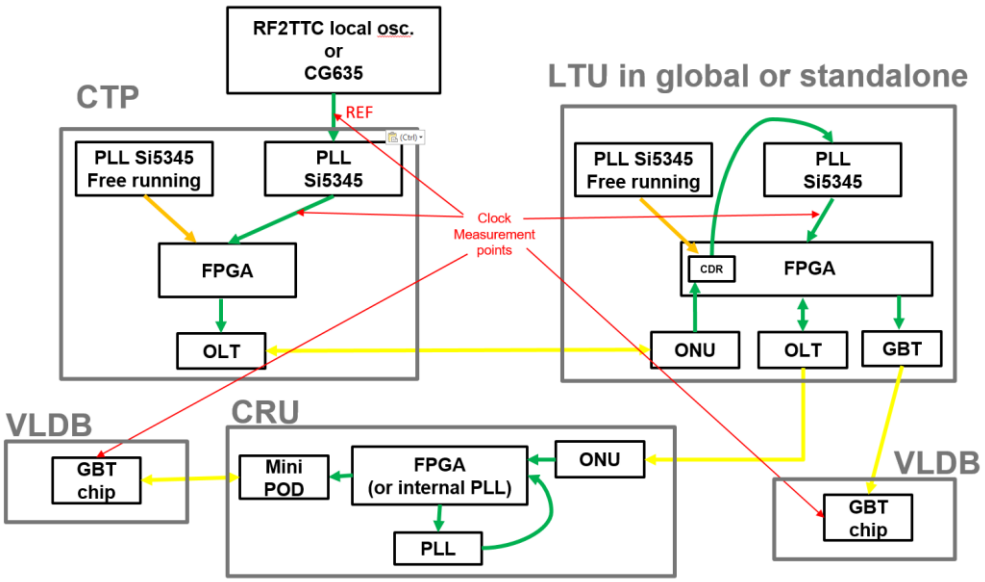

Figure 2. Layout of components for clock phase stability test. Yellow connections are optical and green are electric, synchronized to the LHC clock. The orange connection denotes an electric connection from a separate clock, not synchronized to the LHC clock.

3 Summary

A new ALICE trigger system for Run3 has been proposed and developed. Tests of a laboratory system analogous to the full ALICE system were presented. The temperature dependence of timing parameters of the system was measured. The results of the test indicates that the system fulfil required specifications.

The tested boards will be given to the detector laboratories with appropriate firmware and software and will be used to integrate these into their systems. The second production phase will be initiated in autumn of this year.

Figure 3. Clock phase stability at 35 deg. C for the CTP-LTU-VLDB chain. (See text.)

References

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