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Radiation hardness test of the nSYNC ASIC with 60 MeV proton beam

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The nSYNC chip is a radiation tolerant custom ASIC, developed in UMC 130 nm technology for the upgrade of the readout electronics of the LHCb Muon System. The chip will work, over ten years of upgrade operation, in a radioactive environment and exposed to a total dose of 13 krad and a fluence of $2 \cdot 10^{12}$ cm^{-2} 1-MeV neutrons equivalent. The results of radiation tests performed at the Catana facility (INFN - Laboratori Nazionali del Sud) with 60 MeV proton beam are discussed, with a particular focus on the internal logic and TDC performance, and Single Event Effects measurements.

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1. Introduction

The LHCb detector is a forward spectrometer at the Large Hadron Collider (LHC) at CERN, optimised to perform precision and exploration studies on heavy flavour physics. In the 2019-2020 period an important upgrade of the detector is foreseen to allow the increase of the instantaneous luminosity to $2 \cdot 10^{33}$ cm^{-2}s^{-1} [1]. To overcome the severe limitation of the current hardware trigger, a completely new design of the readout system is necessary to run trigger-less at 40 MHz.
In particular the current SYNC chip, the main component of the readout of the muon system, will be replaced by the nSYNC, a new radiation tolerant custom ASIC developed in UMC 130 nm [2], which implements all the readout functionalities required for the upgrade operations.
The chips will be located in boards in off-detector racks, far from the interaction region. Nevertheless, due to the increased luminosity, the radiation levels are not negligible and an assessment of the nSYNC performance under radiation is necessary, to ensure the proper functionality in upgrade conditions.
According to FLUKA radiation levels simulations, in the highest activity positions a Total Integrated Dose (TID) of 13 krad is expected, after 10 years of upgrade operation. The expected fluence values are $2 \cdot 10^{11}$ cm^{-2} hadrons with energy greater than 20 MeV, and $2 \cdot 10^{12}$ cm^{-2} $1-$MeV neutrons equivalent. A safety factor 2 has been applied to these values.
The irradiation tests were performed up to 120 krad, about 10 times the expected dose, with a full characterisation of the main functional blocks of the chip.

nSYNC architecture and radiation hardness

The main purpose of the nSYNC is to time align digital data arriving from front-end electronics, corresponding to hits in the muon chambers, tag them with the bunch crossing identification number and finally format and send the information out through 14 LVDS links. In each of the 48 input channels the signal arrival time is measured by a TDC, which uses a fully digital DCO and is equipped with a dithering correction system [3]. The TDC can work with several time resolutions, i.e. the number of slices the clock can be divided in, from 8 to 32. A histogram facility for the time measurements is also present for each channel.
To mitigate SEU errors two radiation hardness techniques were implemented: Triple Modular Redundancy (TMR) and Hamming coding. The most critical registers, those for configuration and for the processing of synchronous commands from the LHCb central readout system, are protected by TMR. The number of SEUs detected by TMR is stored in a specific internal counter.
The internal read-only counters and buffers and the TDC Finite State Machine (FSM) states are instead protected by the Hamming parity check code. The digital words are extracted by the Error Detection and Correction logic (EDAC), which is able to detect one or two errors and correct it in case of single error. Also in this case the number of detected and corrected errors are stored in particular read-only registers. Other read-only registers, like histogram ones, are not protected.

2. Irradiation with protons

The irradiation tests were carried out with proton beam at the Catana facility, a clinical proton therapy center at the INFN Laboratori Nazionali del Sud, in Catania (Italy) [4]. The protons'

energy is 62 MeV and the flux provided is $5.7 \cdot 10^8$ protons /cm^{2}s. The corresponding Linear Energy Transfer (LET) is about 9 MeV cm^2/g.
A 15 mm diameter collimator was used to define the beam spot, allowing an accurate estimation of the fluences, thanks also to the Catana beam current monitoring.
Various Printed Circuit Boards (PCB) were built to host the nSYNC chip, soldered to the board, the power supply interfaces, both for Input/Output (I/O) at 3.3 V and the chip core at 1.2 V, the output for LVDS signals and the I^{2}C interface, used for setting configuration and monitoring. The boards are also equipped with different pins to monitor internal signals, i.e. the 40 MHz clock was continuously monitored by means of an oscilloscope.
Three chips in total were tested under the same conditions in order to compare the results. The test boards were located at about 10 cm from the collimator, and aligned with an optical system.
A complete custom data acquisition system was developed, with a unique centralised LabVIEW software to remotely control and monitor the oscilloscope and the power supplies, in order to detect Single Event Latchups (SELs), and to automatise I^{2}C communication to detect and count SEUs, both in protected and non-protected chip blocks.

2.1 Tests description and results

For each chip, the test was divided in seven subsequent runs. In the first five runs the beam intensity allowed a TID of 8 krad per run, integrating 40 krad in total and an overall fluence of $3.7 \cdot 10^{11}$ p. cm^{-2}. The other two runs were taken at 40 krad per run. Hence, a final TID of 120 krad and a fluence of $1.1 \cdot 10^{12}$ p. cm^{-2} was reached. In the seventh run the dose rate was increased by an order of magnitude, from 8 rad/s to 80 rad/s.

2.1.1 Current consumption

The typical nSYNC current values for the I/O interface are comprised between 80 and 120 mA, depending on the LVDS output load, and about 30 mA for the chip core. The currents remained stable during the irradiation test, with no abrupt increase, neither soft SEL, for each chip tested. A small increase was observed on the I/O current, during the low dose rate (8 rad/s) test, of 0.8% in one equivalent LHCb upgrade (i.e. ten years of operation), as shown in Fig.1 (left). In the last run, at higher dose rate, a constant current rise of 1.2% was observed. Overall, a total increase of about 20% was observed with respect to the original value before the irradiation. These cumulative effects are also compatible with those obtained from independent test using X-Ray radiation.

2.1.2 TDC performance

To test the TDC performance with respect to TID, in absence of front-end input signals, the internal automatic DCO calibration procedure was instead used.
Having chosen a particular TDC resolution, a calibration signal is generated internally at the beginning of the 40 MHz clock cycle and the DCO control word is found using a SAR (Successive Approximation Register) approach. Subsequently the direction and the value of the dithering correction are calculated.
The corresponding DCO values are stored in read-only registers, which were read back through the I^{2}C bus at each run start. The values as function of the resolution chosen and channel number, at increasing TID, were then studied offline. The curves are super-imposable with no evident trends

at increasing TID. At the LHCb nominal resolution (16), the points tend to higher DCO values after the first irradiation step, as shown in Fig.1 (right), but this effect is within the dithering correction, thus is negligible in terms of time measurement.

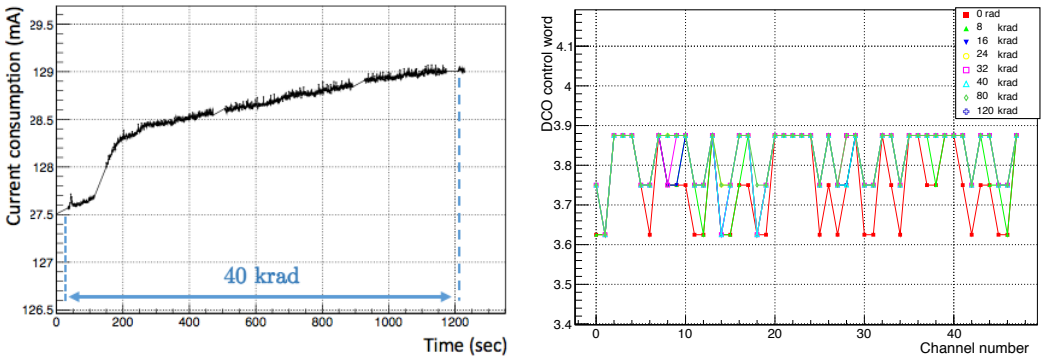

Figure 1: Left: I/O current increase during the first run for the first chip tested. Right: TDC DCO control word at resolution 16, as function of channel number and TID.

2.1.3 PLL and LVDS jitter

The clock generated by the PLL was monitored to measure the possible jitter increase with respect to the integrated dose. The same measurement was done on one LVDS output, sending a periodic signal to the output interface. No instability or abrupt behaviour for both signals was observed during the full test and for all chips, neither any cumulative effect. A rise in the PLL jitter of about 2 ps, corresponding to $\sim 5\%$, was observed strictly limited to beam presence. The LVDS signal jitter did not show an increasing trend but only fluctuation of about 4%.

2.1.4 SEU studies

The number of SEUs was measured reading periodically the nSYNC registers through the I^2C interface, in particular counting the bin-flip occurrences and reading the internal error counters. Knowing the fluence values at each end of run, the SEU cross section per functional block, σ_{SEU}, can be obtained from the angular coefficient of a linear fit on the number of observed SEUs with respect to the fluence, hence taking into account possible statistical fluctuations and checking the stability of the cross section itself, as shown in Fig.2. All the σ_{SEU} measurements were consistent for all the chips tested.

For each input channel, after the DCO calibration, the TDC status is stored in 2-bytes wide unprotected registers, which were readout periodically every second. An SEU is then immediately observable as a permanent bit-flip. The average cross section for these registers (90 bytes) is $5.8 \cdot 10^{-11}$ cm^2. The corresponding expected error rate for the whole LHCb muon system is thus 1.8 events/day, with no effect whatsoever in the LHCb data quality.

The same measurement was performed for the histogram registers (2.3 kbytes), shown in Fig.2, which values were downloaded every 2 minutes, and resulting in an average cross section of $0.9 \cdot 10^{-9}$ cm^2, corresponding to ~ 30 events/day for the whole muon system. Since the histogram facility is used only for time alignment purpose and not during normal data taking, this rate has no practical effect on LHCb normal operations. The SEU measurements were done also for the

functional blocks protected by TMR (195 bytes) and EDAC system, reading continuously internal counters. The TMR system never failed the correction: this corresponds to a detected SEU cross section of $8 \cdot 10^{-11}$ cm^2, and an upper limit of $8 \cdot 10^{-13}$ cm^2 for the not corrected one. SEU on EDAC protected regions were not corrected only if occurred as double errors in a digital word, situation observed in less than 3% of the total number of detected errors, corresponding to a detected SEU cross section of $13 \cdot 10^{-11}$ cm^2, and an actual error cross section of $4 \cdot 10^{-12}$ cm^2. The related expected error rate is 0.1 events/day for the whole muon system.
For TDC status, histograms and TMR-protected blocks, a normalization to the overall number of involved bits was calculated, in order to check the consistency of the different cross section results and to get a more technology-specific quantity. The values are all compatible for each nSYNC functional blocks considered: the final SEU cross section per bit is $(0.6 \pm 0.1) \cdot 10^{-13}$ cm^2.

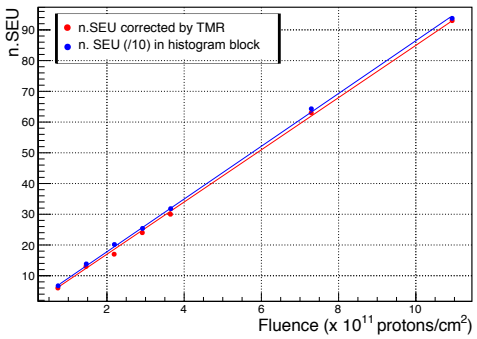

Figure 2: Number of SEUs with respect to fluence for the first chip tested. In red, SEUs detected and corrected in the TMR-protected registers. In blue, SEUs occurred in the histograms registers (the y axis scale must be multiplied by 10).

3. Conclusions

In the irradiation tests at low LET (9 MeV cm^2/g) using 60 MeV proton beam the nSYNC showed an excellent performance, with no failure behaviour or SEL after a TID 10 times larger the one expected in 10 years of LHCb upgrade operations, and a chip current increase below 1% and a clock jitter variation not larger than 5% in one equivalent LHCb Upgrade. The SEU cross section per bit was also measured to be $(0.6 \pm 0.1) \cdot 10^{-13}$ cm^2. Further tests at higher LET for UMC 130 nm technology will be important to determine the SEU saturated cross sections and investigate LET thresholds.

References

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