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Control and Monitoring for a serially powered pixel demonstrator for the ATLAS Phase II upgrade

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The Inner Tracker (ITk) is a new, all-silicon detector under development for the ATLAS Phase-II upgrade and will operate at the High Luminosity LHC. A serial power (SP) scheme will be used for the ITk Pixel Detector. New elements are required to operate and monitor a serially powered detector, including a Detector Control System (DCS), constant current sources and front-end electronics with shunt regulators. A demonstrator for the three outer barrel layers of the ITk Pixel Detector is being built at CERN to verify and qualify the SP concept, and to gain experience operating a SP chain. It includes all required elements for controlling and operating SP chains safely, from an interlock system to in-situ monitoring with a new DCS. A first full electrical prototype with seven quad modules was successfully tested. This prototype includes pixel modules, the DCS elements, realistic services and can be read out by different data acquisition systems. Problems identified during the commissioning and operation of the small electrical prototype went into the requirements for the future front-end (FE) chips. Many institutes worked on the development and integration of the individual parts. Further and longer chains are under construction and will allow tests of multiple SP chains mounted on the same local support in parallel. It is also foreseen to operate a SP chain with 16 modules.

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1. Introduction

Serial power is the baseline scheme for the Pixel Detector in the Inner Tracker (ITk), aiming to reduce the amount of services and material[1]. A new Detector Control System (DCS) is required to monitor and control the serial power (SP) chain. A full system setup was assembled to test all elements in a SP chain together. Section 2 describes the system test infrastructure and prototype. The DCS concept implemented in the setup is explained in section 3. Experiences from the operation of a SP chain with seven quad modules are given in section 4.

2. Outer Barrel Demonstrator

The demonstrator program for the outer barrel pixel detector aims to assemble a fully-functional prototype including required infrastructure for testing the full system. It implements a system design and layout solution for the three outermost layers of the ITk Pixel Detector. Not all components are in their final form but still allow for gaining experience in building and operating larger systems, and performing system tests with various prototypes.

Within the demonstrator program, several prototypes which are designed to investigate different aspects of the system like mechanical integration, thermal performance and full electrical systems, are being built. The final demonstrator will include multiple SP chains with inclined dual (two FE) and flat quad (four FE) modules mounted on one cooling pipe. In total there will be 120 FE-I4 chips. The FE-I4 is a readout ASIC developed for the insertable innermost pixel layer [2, 3]. This readout chip already includes a shunt regulator required for operation in a SP chain. This paper focuses on a small electrical prototype currently in operation.

2.1 Serial power

In a SP chain the current flows through the modules in series. Figure 1 shows the block diagram of the SP used in the demonstrator.

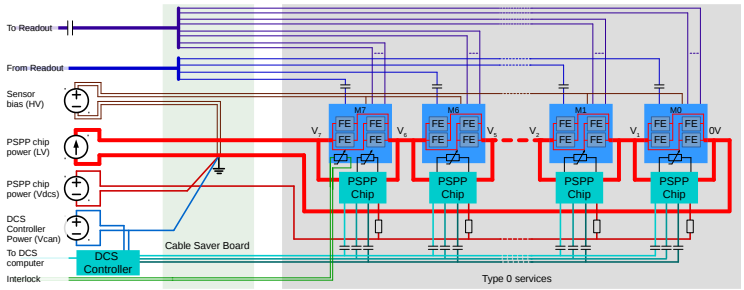


Figure 1: Block diagram of the SP chain used in the demonstrator.

The four FEs in a quad module are operated in parallel. The FE uses a shunt LDO regulator [4] which stabilizes the voltage across the module, and shunts additional current required to operate with a constant current. The parallel use gives redundancy in case of a regulator failure, as the regulators can shunt additional current taking over the load of the failing regulator. A further protection is the Pixel Serial Power Protection (PSPP) chip. This ASIC is connected in parallel to the module. It includes a bypass transistor that can short a faulty module in the chain [5].

AC coupling is required for the communication with the FE and PSPPs chips.

2.2 Small electrical prototype

The full demonstrator is still under construction. A small electrical prototype with one SP chain of seven quad modules was built (see Figure 2) and tested to verify the concept. As planned for the full demonstrator, it contains all components foreseen in the final system. The services to power the modules are realized with flexible PCBs, one for the data and one for the power lines. Both are integrated in the mechanical structure and are connected to a cable saver board. The PSPP is mounted directly on the power flex allowing the SP chain to recover if a connector fails. A common ground for all powering (sensor bias, module and DCS power) is on the cable saver board.

Each module was tested individually before integration onto the mechanical support. This allowed for a comparison to verify whether the operation in the SP chain changes its characteristic.

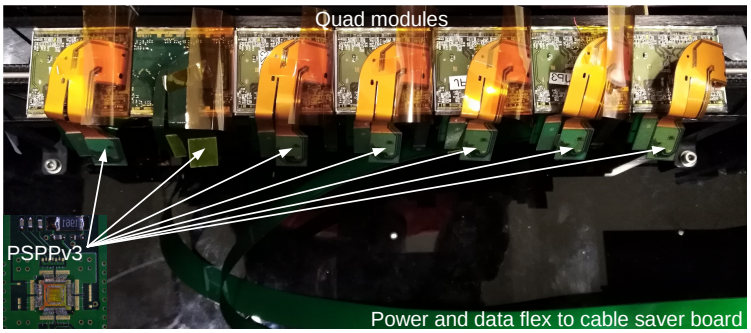


Figure 2: Small electrical prototype with a seven quad-module SP chain.

3. Detector Control System

The demonstrator includes all elements of the DCS as described in reference [6]. It is based on three paths with increasing granularity: 1. Interlock, 2. Control and 3. Diagnostics. Figure 3 shows the different elements of the DCS.

The diagnostic path is not yet integrated into the demonstrator, as it is not properly supported by the FE-I4 chip and because multiple readout systems are tested with the demonstrator. It is foreseen that the final readout ASIC sends status information along its data path which is delivered to the DCS for diagnostic purposes.

3.1 Control and monitoring

The main element of the control path is the PSPP chip. This chip measures the temperature and voltage of the module and it includes the bypass mentioned above. The PSPP communicates through the slow control bus (SCB). This bus was developed to handle a single ended communication with AC coupling. The prototype chip PSPPv3 is used in the demonstrator [5]. This chip includes all required functions.

The DCS controller acts as master of the SCB and is the bridge to the computer. Currently an FPGA is used because the DCS controller ASIC is still in development. The control path is intended to be available all the time including when the FEs are switched off. This allows for monitoring of the detector status during possible annealing times and long shut downs.

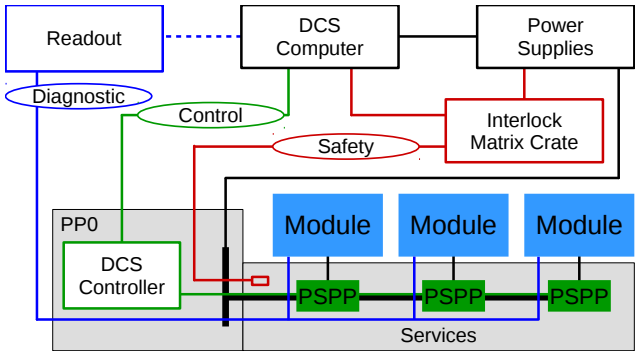


Figure 3: Concept of the DCS with the three independent paths.

3.2 Interlock

The Interlock path is a last line of defense. It is a purely hardware based system which requires no configuration and protects humans and the detector. The granularity of the interlock is per SP chain as it acts directly on the power supplies. For debugging purposes, all interlock sensors are monitored independently of their interlocking function.

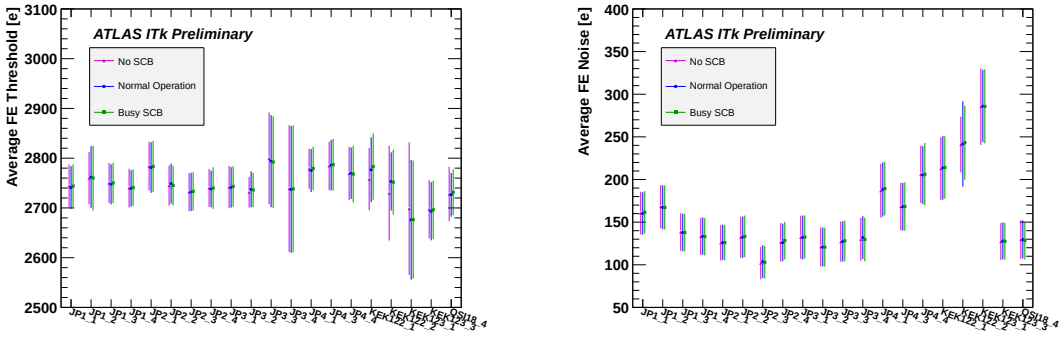
The main element of the interlock system is the interlock matrix crate (IMC). This crate was originally developed for the insertable innermost pixel layer and is a modular system that uses a CPLD as main logic element [3]. The crate was modified for the demonstrator. It checks the temperature, dew-point, switches and light sensors to verify that the setup box is closed. Additionally the crate has a connection to the cooling plant.

4. Experience from the operation

The supervisory control and data acquisition tool (SIMATEC WinCC Open Architecture [7]) allows to log and collect all DCS sensor values coming from the interlock and control path. Having all information available was very useful in commissioning and debugging the seven module structure. Furthermore it is possible to check the status of the setup remotely.

The module voltage measured by the PSPP allowed for identification of modules in the chain which were not properly configured. The experience from the demonstrator was also directly fed into the requirements of the ITk production FE chip to prevent observed failure modes in the final FE ASIC, e.g. FE ignores random signals on the command line. Similarly, problems found in the PSPP could be corrected in a new version, e.g. disabling of data output line, when no clock is present at power-up.

A threshold scan was performed with different activities on the SCB to verify if additional noise is created by the SCB. The cable was unplugged to have a reference with no activity. A second measurement was performed with regular activity and a third with very high activity. The results of the measurements are shown in Figure 4. The figure shows the tuned threshold and noise for each front end individually. There is no significant variation between the three measurements for all FEs. Note that the modules used were left over modules which are not perfect and thus some variation is seen between the FEs. The modules JP4 and KEK122 could not be biased resulting in the higher noise. It can be concluded that the SCB does not add measurable noise into the system.



(a) Threshold (b) Noise

Figure 4: Results from the threshold scan to measure noise induced by the SCB.

5. Conclusion and outlook

The demonstrator program is a successful collaboration between many institutes. It was possible to test many integration steps and bring together all required elements. The small electrical prototype gave first experiences with a realistic SP chain. It allowed us to better understand the requirements for the power supplies and identify problems within the components which can be corrected in future versions. Further tests with the bypass are planned together with a current source prototype. With the full electrical demonstrator it will be possible to test a SP chain with 16 modules and operate multiple chains in parallel.

Acknowledgments

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