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The Proton Timing System of the TOTEM experiment at LHC

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The TOTEM experiment has developed a new timing detector to be used during a special LHC run. The new proton timing detector, based on Ultrafast Silicon Detectors, is installed in the TOTEM Roman Pots, at 220 meters from the interaction point 5 at LHC. The sensors are readout through a fast sampler chip: the SAMPIC. With a sampler, it is possible to record the detector waveforms so that sophisticated offline algorithms can be used to achieve the best timing performance. A new board has been designed to integrate the chip in the TOTEM and CMS DAQ and control systems. The core component of the board is a radiation hard FPGA, with a dedicated firmware designed to configure the SAMPIC and assemble the DAQ data frame event. The system was successfully operated during the run in July 2018. The detector will be described and the preliminary results discussed.

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1. Introduction

TOTEM is one of the experiments of the LHC, located at the interaction point 5, together with the CMS experiment. The TOTEM experiment is focused on diffractive processes, which include elastic scattering, single, double and central diffraction, where one or both hadrons can survive the interaction and be scattered in the very forward region. Such protons are eventually detected by the sensors hosted in the TOTEM Roman Pots (RPs), symmetrically located at more than 200 m from the interaction point. The RP is a secondary vacuum vessel, which can host different types of detectors, that can be moved into the primary vacuum of the machine through vacuum bellows. The detectors can thus approach the beam down to few millimeters, which allows scattered protons to be detected and measured down to few microradians.

The capability of performing common data taking with the CMS experiment opens up to the possibility to perform detailed studies of central diffractive (CD) processes[1], where both protons stay intact and a rapidity-isolated system X is generated in the central region instrumented by CMS. The possibility of proton tagging leads to an exceptional background reduction and studies of exclusive processes. Using a dedicated LHC optics (magnet configuration) with an amplitude function $\beta^* = 90$ m, which is larger than the one used for standard LHC runs, it is possible to perform studies on low central diffractive masses ($M_X \sim$ 1-3 GeV/c^2). Low mass spectroscopy and studies of glueball candidates can be carried out in such conditions. The physics program has been already exploited with a run performed in 2015 ($\sim$0.4 pb^{-1} collected), but more statistics are needed.

To collect the needed statistics the highest possible luminosity with a $\beta^* = 90$ m must be reached. This has the drawback of an increased pile-up, represented by simultaneous pp interactions in the same bunch crossing. To disentangle the detected protons and perform a precise event reconstruction, four additional RPs have been equipped with new very precise timing detectors, with a target timing resolution ≤ 50 ps. Therefore it is possible to reconstruct the longitudinal coordinate of the protons at the interaction point by measuring the difference of the proton arrival times in the two detector arms.

2. UFSD Timing sensors

The sensors used in the timing system are Ultrafast Silicon Detectors (UFSD[4]), based on low-gain avalanche diode optimized for timing measurements. Each sensor is divided in 12 pixels of different sizes, optimized to have the same occupancy. UFSD sensors are glued and bonded to the TOTEM hybrid board, which provides 12 dedicated amplification chains, one for each channel. The hybrid, originally designed for scCVD diamond sensors and better described elsewhere [3], was modified to amplify UFSD signals. The amplification is made of two stages, with 3 active elements (one BFP840ESD and two BFG425W BJT transistors). Results obtained in test beam with the board prototypes have shown a time precision in the range 30-100 ps [5]. The time precision scales, as expected, as a function of the pixel capacitance, which varies in the range 3-28 pF, almost linearly with the pixel area (coefficient $\sim$ 2pF/mm^2). The rise time of the signal has been measured in the range $\sim$ 0.7-1 ns, with a SNR[1] in the range 30-50 and a mean amplitude $\sim$400 mV. The

[1] Signal to Noise Ratio (SNR) is defined as the ratio between the signal amplitude and the noise RMS.

hybrid has been designed to be as thin as possible, so that four detection planes can be hosted in a single RP, enhancing the final resolution by a factor 2 w.r.t. a single layer configuration. The final resolution is thus expected to be better then 50 ps (and much better in the area close to the beam, where the smallest pads are placed) for all the pixels. The full system has a total of 192 timing channels, with 16 UFSD sensors (4 RPs).

3. Sensor Readout

To perform the sensor readout we developed a strategy based on a fast sampler, the SAMPIC chip[6]. The SAMPIC is a 16 channel ASIC, operating as a fast sampler of the analog input signals. For the special run we operated the chip at a frequency of 7.8 GSa/s. The input range is $\sim$ 1 V (single-ended) with a 1.6 GHz bandwidth, well matched with the signal characteristics.

Each SAMPIC channel is self-triggered by an internal discriminator on the input and digitized independently from the others. The order in which triggered channels are readout is random, without time sorting, and the event building based on the central trigger must be done elsewhere. To reduce the data payload and minimize the channel dead time (down to 250 ns, independent for each channel) we decided to operate the SAMPIC at 8 bit resolution and to collect only 24 samples for each waveform (out of a maximum of 64). An overall acquisition window of 3.1 ns was provided, granting the sampling of the signal pedestal, very valuable for offline corrections, and the full rising edge of the signal. The signal maximum is identified and recorded as well.

The SAMPIC chip is mounted on a SAMPIC mezzanine board developed in Saclay. Two SAMPIC mezzanines can be plugged in the Digitizer Board (figure 1), a joint project of TOTEM and CMS, used also in the PPS project[2] . The board is based on the Microsemi SmartFusion2 FPGA, an high performance FPGA protected against single event upset. It hosts multiple mezzanines and interfaces the two SAMPIC chips with the TOTEM/CMS readout and control systems. Data are sent to central CMS DAQ through dual optical link (GOH [7], 800 Mb/s each channel). Slow control and fast commands (like trigger) are handled by the Communication and Control Unit (CCU). An USB connection (QuickUSB [8]) is also present for test beams and debugging.

The DAQ requires that one and only one data frame is generated for each trigger (L1A), with a maximum L1A rate of $\sim$ 100 kHz and 6 μs latency. Moreover frame payload must be limited to $\sim$ 350 Byte/chip, one of the major constraint of the design. The firmware handles the configuration of the SAMPIC mezzanine and perform the packet selection (one packet contains the info about one digitized waveform), the DAQ frame building and the data compression (see fig.1 for a scheme). The synchronization unit is the module which provides the synchronization of the SAMPIC data with the experiment DAQ and handles internal clock domain crossings. For each L1A received a timestamp TS is created by subtracting the trigger latency (remotely controlled) from the trigger arrival time. When a waveform is digitized in a SAMPIC the relative data packet is sent to the FPGA. With a real-time algorithm the SAMPIC timestamp is reconstructed and checked against all the TSs generated. Only matching packets are accepted and sent to a channel dedicated FIFO, after an integrity check. A data reduction $\sim$ 10 is achieved at this stage. The Frame Builder module reads the first TS still waiting for building and collects all packets in the channel FIFOs with the matching timestamp , assembling the final event frame. Further data compression and zero suppression are performed at this stage. To fit the data stream size a limit (software controlled) on the maximum

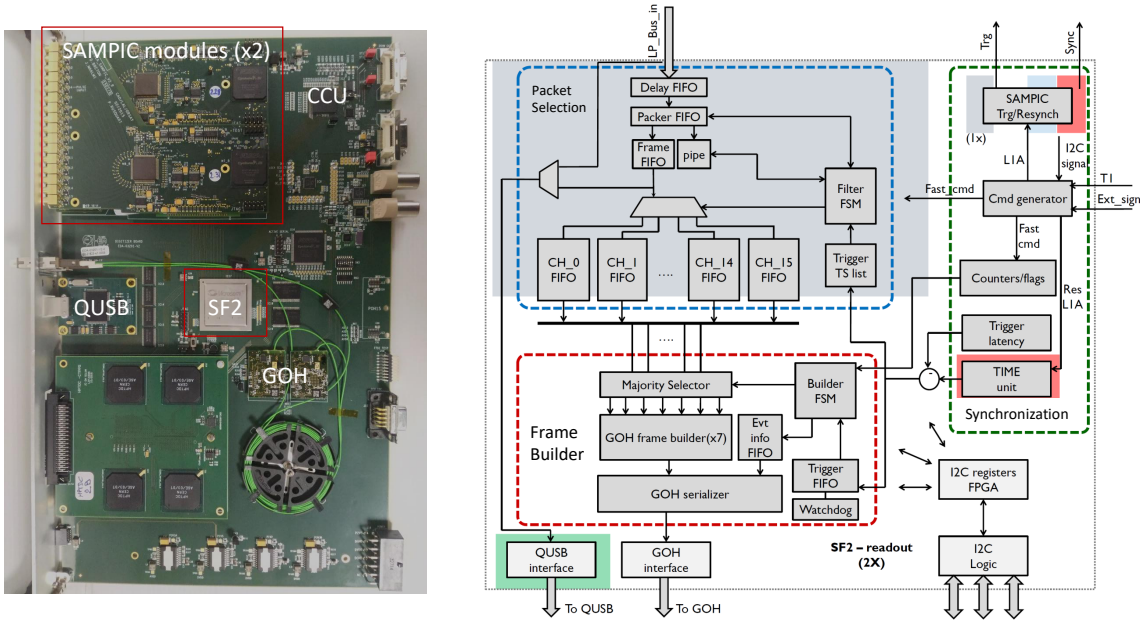

Figure 1: On the left a picture of the Digitizer Board fully equipped. A second mezzanine is present at the bottom of the board, hosting the TDC chips used in the PPS project. On the right a scheme of the readout section of the firmware developed for the SF2 FPGA.

number of waveforms to be transmitted for each event is defined. Not transmitted channels are flagged in the data stream. During the run, flags were online monitored to check the transmission efficiency and optimize the limits. The frame is finally sent to the DAQ system.

4. Preliminary results

The system was successfully and continuously operated during the five days of data taking (July 2-7 2018). The final recorded integrated luminosity was $\sim$5.6 pb^{-1}. Preliminary results show that the collected waveform are of high quality. In figure 2 (right) a typical waveforms is displayed. Offline ADC calibrations (to be applied not only channel by channel, but also sample by sample) have been successfully applied, enhancing the overall time resolution of the system. The maximum number of waveforms to be transmitted for each event was optimized independently for each board. The achieved transmission efficiency was above 99% for almost all channels (fig.2, left). Some channels were masked due to noisy pixels.

Studies of efficiency and timing performance are ongoing and results will be available soon. While some planes have poor efficiency, the presence of 4 detection planes in each RP nevertheless can permit the system to reach the desired timing resolution. The high-efficiency planes have timing resolution in line with the previous test beam results. Efficiencies have been measured using the tracking detector as reference.

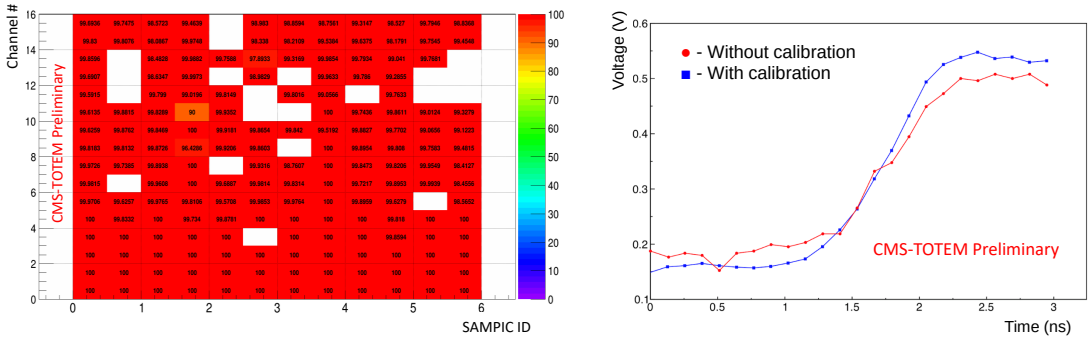

Figure 2: On the left the transmission efficiency for all the channels. On the right an example of waveform, before and after the offline calibration procedure.

5. Conclusions

Timing stations with a resolution in the range 30-100 ps based on UFSD sensors have been realized for the TOTEM-CMS special run. Readout is done through the SAMPIC chip, a fast sampler. A dedicated firmware and digitizer board have been developed to integrate the chip in the TOTEM-CMS environment. The timing system has been operated without any interruption during the special run in July 2018, where an integrated luminosity of $\sim$5.6 pb^{-1} was recorded. Collected waveforms show a good quality and the system was able to respect the DAQ bandwidth with a transmission efficiency above 99%. Data collected during the special run are under analysis and first results on detector timing performance will be soon available.

References

[1] G. Antchev et Al. (TOTEM coll.), Timing measurements in the Vertical Roman Pots of the TOTEM Experiment TDR. CERN Technical Disign Report, CERN-LHCC-2014-020, TOTEM-TDR-002.

[2] CMS and TOTEM collaborations, CMS-TOTEM Precision Proton Spectrometer. CERN Technical Disign Report, CERN-LHCC-2014-021, TOTEM-TDR-003, CMS-TDR-13.

[3] G. Antchev et Al. (TOTEM coll.), Diamond Detectors for the TOTEM Timing Upgrade. *JINST* **2017**, *12 03*, P03007, 10.1088/1748-0221/12/03/P03007.

[4] H.F.-W.Sadrozinski et Al., Sensors for ultra-fast silicon detectors. *NIMA* **2014**, *765*, pp. 7-11, 10.1016/j.nima.2014.05.006.

[5] R. Arcidiacono et Al., Test of Ultra Fast Silicon Detectors for the TOTEM upgrade project. *JINST* **2017**, *12 03*, P03024, 10.1088/1748-0221/12/03/P03024.

[6] E. Delagnes et al., The SAMPIC Waveform and Time to Digital Converter. *IEEE Nuclear Science Symposium and Medical Imaging Conference* **2014**, United States, 10.1109/NSSMIC.2014.7431231.

[7] J.F.Grahl, Optical Data Links in CMS ECAL. *10th Workshop on electronics for LHC experiments* **2005**, Boston, USA.

[8] Bitwise Systems, QuickUSB User Guide. Web page:http://www.bitwisesys.com/v/public/media/quickusb user guide v2.11.41.pdf