Test Strategy for Low Failure Rates and Status of a Highly Integrated Readout Chip for PMTs in JUNO

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The Jiangmen Underground Neutrino Observatory (JUNO) is a multi-purpose experiment with the neutrino mass hierarchy determination as main objective. The signal detection is based on a 20 kt liquid scintillator surrounded by photomultipliers (PMTs) that are read out with electronics close to them. A highly integrated analog to digital conversion unit with low power and large dynamic range is developed in 65 nm CMOS to be integrated into the PMT housing. Due to the inaccessibility of the electronics, low failure rate has to be achieved. A rigorous production test strategy is developed and presented here to increase the test coverage and effectively eliminate the expected failure rate in the experiment's runtime. This work also gives an overview of the features and some recent measurement results from the second generation of the readout chip.

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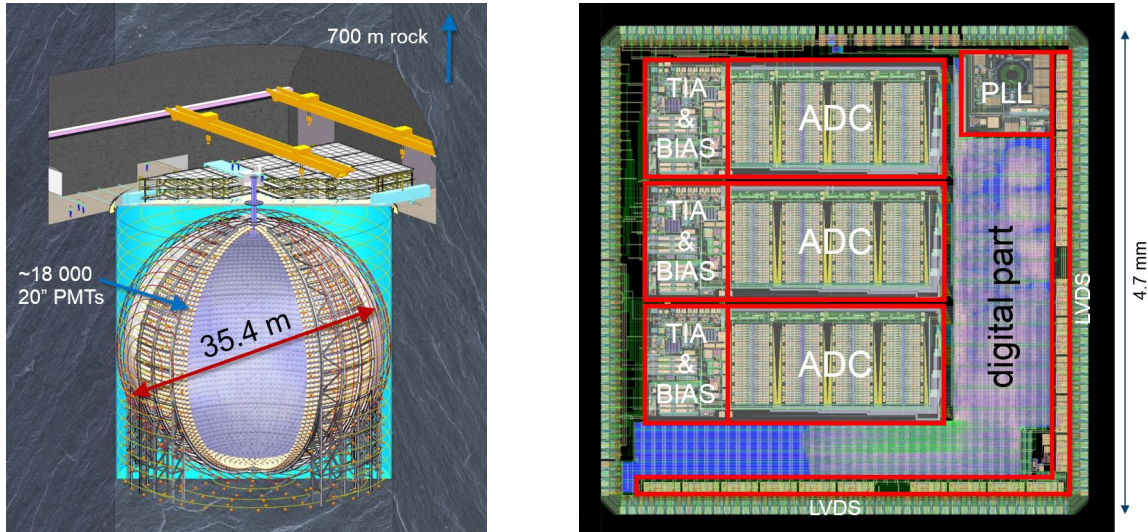
Figure 1: *Left:* The underground central detector of the JUNO experiment showing the submerged sphere with the surrounding photomultiplier tubes [2]. *Right:* The layout of the Vulcan chip with the three receiver chains in the top left, the clock generation in the top right and the digital part on the right and lower edges.

1. Introduction

The integrated circuit discussed in this paper is developed for the Jiangmen Underground Neutrino Observatory. It is an upcoming multi-purpose neutrino detector under construction in China with the primary focus on determining the neutrino mass hierarchy. Its location is chosen to be both with equal distance of two nearby nuclear power plants and with a significant rock overburden of 700 m to achieve a good suppression of background radiation. The first data is planned to be taken in 2022 with a subsequent runtime of 6 years [1].

The central detector is a sphere filled with 20 000 t liquid scintillator as an active volume and submerged in water to support the weight, see Figure 1, left. The sphere is surrounded by roughly 18 000 photomultiplier tubes (PMTs) with a diameter of 20 inch. For the discussed readout chip, the electronics is aimed to be integrated into the PMT housing to preserve signal quality and reduce the number of cable connections. Besides biasing of the PMT itself and general control, the electronics consists of a data processing system around an analog to digital unit (ADU) as central component.

The water-tight assembly and inaccessible mounting of PMTs for maintenance requires highly-reliable readout electronics that contribute to a maximum of 0.5 % failed channels during the lifetime of the experiment. After giving an overview of the ADU design, the developed test strategy is presented to minimize the contribution of the ADU to channel failures.

2. The Vulcan Chip

The presented chip, called Vulcan[1], is a proposal for the ADU and is a widely configurable, complex system-on-chip (SoC) in 65 nm TSMC CMOS technology featuring three independent receiver chains with programmable gain. Each receiver chain has an 8-bit flash analog to digital

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[1]*Vulcan* is the son of *Juno* in ancient Greek mythology, hence the name for the chip.
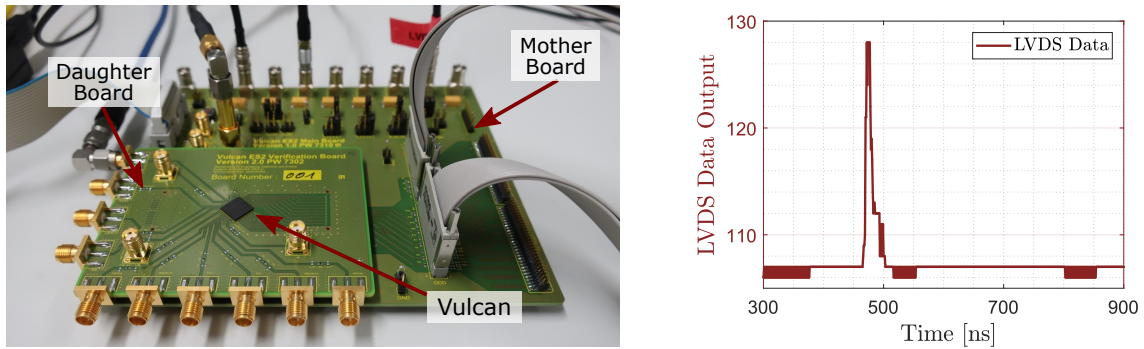
Figure 2: *Left:* The verification board concept is based on two different boards: The smaller one on top holds a packaged and soldered Vulcan sample with dedicated connectors for specific measurements while the bigger one provides all basic connections to the measurement setup common for all measurements. *Right:* The plot shows the ADC output of an exemplary input pulse with a response similar to amplitude and duration of 1 p.e.

converter (ADC) comprised out of four 6-bit sub-ADCs that digitize the data with 1 GSample/s and a signal bandwidth up to 500 MHz. A subsequent digital data processor analyses the current signal and judiciously selects the highest, not-saturated signal with highest gain. This results in a linear voltage input range of more than 80 dB from small signals below 1 photoelectron (p.e.) equivalent charge to above 1000 p.e. [3].

Also embedded on the chip is a low-noise 4 GHz phase-locked loop (PLL) [4] as well as digital control circuitry for automated ADC baseline regulation [3]. Furthermore, three fast trigger lines individual for the three receivers are available to bypass the latency in the internal data processor. The trigger method can be programmed to switch between sample- and integral-based thresholds with the latter integrating the signal over a configurable time. Together, this results in a chip with an active silicon area of $4.7 \times 4.7\,\mathrm{mm}^2$, an equivalent gate count of 1.4 million gates for the digital part and a total power consumption of $\sim 1.2\,\mathrm{W}$. The layout of the second engineering sample can be seen in Figure 1, right, and is in the verification process since its return from production.

The laboratory setup (see Figure 2, left) is built around the packaged Vulcan chip which is soldered on a daughter board specifically adapted for the relevant measurement, for instance with the connections for high frequency input and clock signals or with socket connectors to enable a non-destructive testing of several chips. The daughter board is piggy-back to a mother board with all permanent connections like voltage supplies, configuration interface and digital output lines. Due to the separation into two boards, a quick change in the measurement setup can be performed.

Using this setup, a variety of measurements were carried out, proving the functionality of the chip for both analog and digital blocks. Special attention is put into the ADC as it is the central component for digitization. A comprehensive example is the pulse measurement at full digitization speed of 1 GSample/s shown in Figure 2, right. The input from a pulse generator is configured to give a similar pulse response to that of one photoelectron from the PMT. Noise measurements with an input sine wave at 100 kHz result in a signal to noise ratio (SNR) of 45.92 dB which converts into an effective number of bits (ENOB) of 7.48 fulfilling the required resolution of the experiment translates into $\mathrm{ENOB_{req}} = 7.33$.
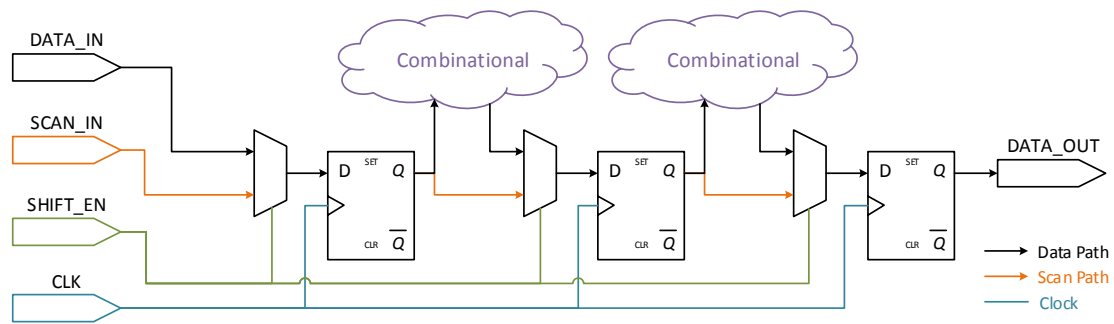
Figure 3: Concept of the scan chain: An additional path is included into the design that enables a preloading of a predetermined logic state into the registers and extracting this state after performing one calculation cycle. In the test, the extracted state will be compared to a reference result to determine any deviations.

3. Test Strategy

As described earlier, the reliability of Vulcan is a key item in the development, hence a strategy has been developed to lower the probability of failures during operation. Failure rates over time can be described with a bathtub curve that shows a higher early failure rate, a stable normal operation time and an increase towards longer operation periods [5]. The latter is dominated by wear-out effects, which can be strongly mitigated through *eletromigration aware design*. Here, metal lines are widened and the number of vias is increased to reduce the impact of material defects due to electron collisions.

With the wear-out-based effects covered by design practices, the remaining failures due to infant mortality have to be detected and filtered out. The failures are generally caused by the production process and may lead to strong and weak defects with different detection strategies.

Strong defects are failures in the circuit that lead to a non-functioning device. A systematic screening procedure can reveal these defects. The *scan chain test* fundamentally provides a high test coverage for digital circuits by adding the possibility to preload the design with a known state, perform the regular operation for a given number of clock cycles and finally readout and compare the state of the design with a reference result. This is achieved by connecting all flip flops additionally into a chain, effectively creating a long shift register (Figure 3). In Vulcan, a scan chain with 25 371 flip flops has been introduced. The subsequent generation of test sequences in an automated test pattern generator provided a test coverage of 91.54 %.

Weak defects on the other hand require a different approach, because initially the functionality is given, however the performance might be affected and wear-out might occur much faster leading to a early failures. A common production fault increases the leakage current by orders of magnitude, thus investigating the current in the quiescent state (*Iddq testing*) may probe with a high coverage of more than 95 % [6]. A further improvement in the fault detection can be achieved by checking the functionality with very low voltage (VLV) tests because the performance of weak devices is affected more severely in this condition [7]. Briefly stressing the circuit with higher-than-normal voltages, a so called *short voltage elevation (SHOVE)* test, continues to increase the test coverage, especially when combined with a subsequent Iddq test [8].

Finally, *measuring key performance parameters* like the frequency of the PLL's oscillator or

gain errors in the ADC enables the sorting of the production lot and exclusion of outliers. Due to the relatively low total number of devices required, a rigorous ratio picking only the best 1/3 of devices is aimed for. This performance screening together with all aforementioned tests should effectively reduce the failure rate of Vulcan chips in the experiment to zero.

4. Conclusion and Outlook

This paper presents the Vulcan chip with a focus on the test strategy towards low failure rates in the JUNO experiment. Motivated from the runtime of the experiment together with the inaccessibility of the readout electronics, special effort has been invested to develop such a strategy. Its primary goal is to filter out weak devices after production which would otherwise lead to early life failures. Wear-out effects are covered by electromigration-aware layout, adding enough margin so that no failures due to the chip itself are to be expected for the runtime.

Prior to the execution of the production test, a rigorous functional and performance testing is done in the laboratory to identify design weaknesses and determine reference values for the screening process. The current status of the tests shows promising results for instance with the effective number of bits of the 8 bit ADC ($ENOB_{meas} = 7.48$) slightly better than required ($ENOB_{req} = 7.33$). Hence, no further iteration is planned as of writing this paper. However, a completion of the performance testing will give a definite answer to this.

5. Acknowledgments

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