

RD53A: a large scale prototype for HL-LHC silicon pixel detector phase 2 upgrades

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The Phase 2 upgrades of silicon pixel detectors at HL-LHC experiments feature extreme requirements, such as: 50x50 μm pixels, high rate (3 GHz/cm²), unprecedented radiation levels (1 Grad), high readout speed and serial powering. As a consequence a new readout chip is required. In this framework the RD53 collaboration submitted RD53A, a large scale chip demonstrator designed in 65 nm CMOS technology, integrating a matrix of 400×192 pixels. It features design variations in the analog and digital pixel matrix for testing purposes. An overview of the building blocks will be given together with test results on single chips.

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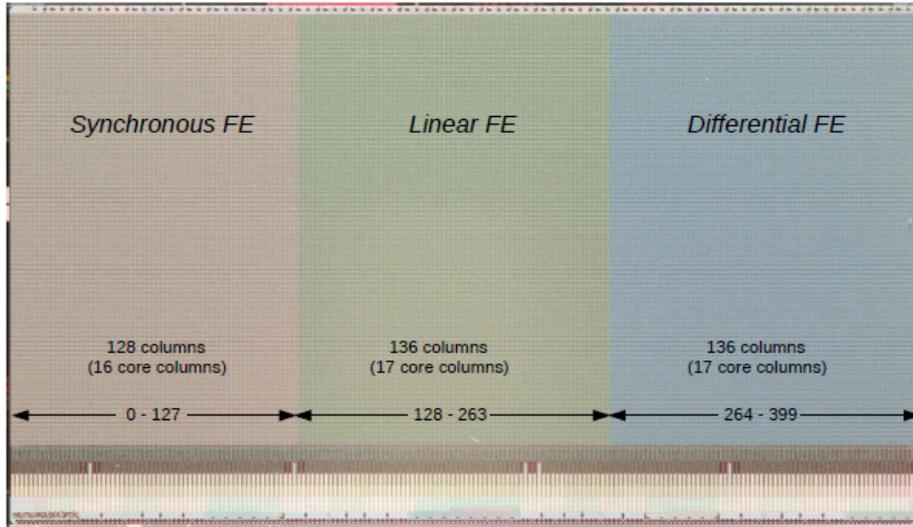


Figure 1: Picture of the RD53A chip highlighting the analog FEs location inside the matrix

1. Introduction

In 2026 the High Luminosity Large Hadron Collider (HL-LHC) will start its operation. From the point of view of the experiments, it will represent a new challenge, notably for the inner tracking systems. Considering the innermost layer, unprecedented level of radiation will be reached (1 Grad in 10 years) together with very high hit rates (around $3 \text{ GHz}/\text{cm}^2$) and readout speeds. These specifications require the design of a new readout chip for the inner tracker silicon pixel detector. For this purpose, the RD53 Collaboration [1] has been established at CERN. A 65nm CMOS technology has been chosen for the design and has been extensively qualified with radiation campaign within the Collaboration, also using dedicated prototypes like the DRAD chip [2]. The final goal of RD53 is the design of a full size pixel chip for the readout of the silicon pixel detectors of ATLAS and CMS. As an intermediate step, the RD53A chip, described in this paper, has been designed. Its purpose is to test the building blocks to be implemented in the final chip.

2. Chip floorplan

RD53A is a $20 \times 11.5 \text{ mm}^2$ chip, featuring a matrix of 400×192 , $50 \times 50 \mu\text{m}^2$ pixels. As it has been conceived as a test chip, it contains design variations in order to characterize them in a large scale prototype. The chip features three flavors of analog front-ends, named synchronous, linear and differential FEs. Figure 1 shows how they are distributed across the matrix. In addition, two digital buffering architectures have been implemented. The Centralized Buffering Architecture (CBA), based on a centralized Time-over-Threshold (ToT) storage scheme, has been integrated with the synchronous FE. The Distributed Buffering Architecture (DBA), featuring a distributed ToT storage scheme, has been integrated with the linear and differential FEs.

Regarding a single pixel, around half of the area is dedicated to the analog front-end and half to the digital logic. The layout of the pixel is conceived so that a square of 2×2 pixels forms a so-called "analog island", in which the 4 analog FE cells are close together and surrounded by digital

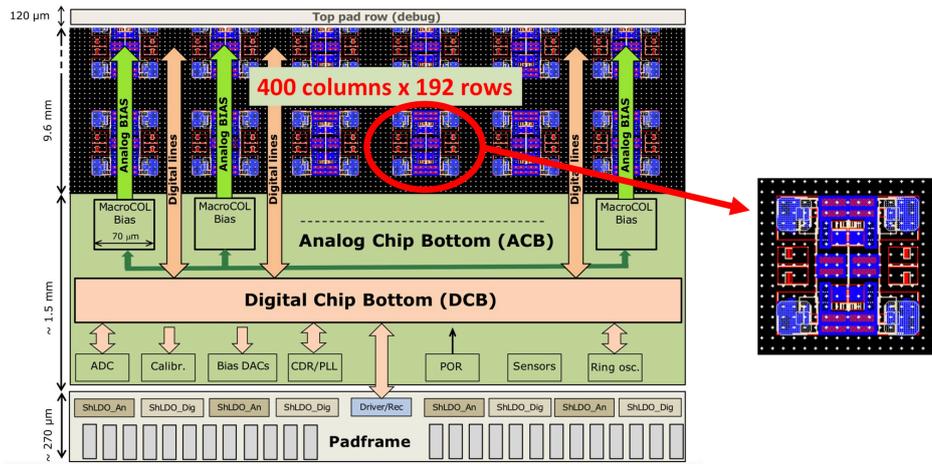


Figure 2: Functional chip floorplan including the view of analog island concept on the right.

cells. This concept is shown in figure 2. As far as the analog part is concerned, this choice allows to provide an optimized isolation from the digital domain, minimizing potential noise injections. 16 analog-islands are then arranged in a 8x8 pixels core, which is the fundamental matrix building block. This layout leads to an optimization of the digital part as well, as it allows a better sharing of logic and buffering reducing the area consumption. This floorplan has been used for all the three analog FEs and the two digital architectures.

As figure 2 shows, the chip periphery is also divided in an analog and a digital domain. The Analog Chip Bottom contains the building blocks required for a proper biasing of the pixel matrix, along with the blocks for voltage and current monitoring, temperature and radiation sensors, clock & data recovery circuit, power-on reset and readout serializers. The Digital Chip Bottom features the blocks concerning the control and readout interfaces. In particular, it contains the channel synchronizer and the command decoder, required to properly configure the pixel matrix. In addition, it features the event builder and the Aurora 64/66b output protocol implemented for the data readout. Lastly, the padframe includes also the Shunt-LDO developed for serial powering.

In addition, a UVM-based simulation and verification environment, named VEPIX53, has been developed within the collaboration [3]. This tool, containing automated verification features, has allowed to perform an extensive comparison between the DBA and CBA architectures and mixed signal tests between analog and digital building blocks.

2.1 Analog Front-Ends

All the three analog FEs included in the chip have been extensively characterized using small prototypes also after irradiation. Notably, the synchronous and linear FE have been included in the CHIPIX65 demonstrator chip and the differential FE in the FE65-P2 chip. Some results regarding the characterization of these prototypes can be found at [4], [5] and [6].

The synchronous FE contains a single stage Charge Sensitive Amplifier (CSA) based on a telescopic cascode scheme. It features a Krummenacher feedback network that provides the sensor leakage current compensation and a linear discharge of the feedback capacitor for ToT computa-

tion. The CSA is AC coupled to a synchronous discriminator, which in normal operation performs the comparison at 40 MHz, corresponding to the bunch-crossing frequency foreseen at HL-LHC. The channel-to-channel threshold dispersion compensation is performed using the capacitors-based autozeroing technique. As a result, no local trimming DAC is needed. In addition, the discriminator can be turned into a local oscillator with selectable frequency, allowing an increase of the ToT computing rate.

The linear FE features a single stage preamplifier based on a folded cascode scheme. It contains as well a Krummenacher feedback scheme for leakage current compensation and linear ToT computation. The first stage is then connected to a high-speed, low power current asynchronous comparator. It performs, together with a ToT counter, the time-to-digital conversion. The threshold dispersion compensation is addressed by means of a local 4-bit binary weighted current DAC.

The differential FE features a 2-stage comparator and a CSA whose input is used as a reference for the comparator's first stage, referred to as the pre-comparator. The CSA contains a constant-current mirror feedback with selectable gain making use of different feedback capacitors. Threshold local tuning is carried out by exploiting one 4-bit resistor ladder in each pre-comparator branch. The pre-comparator stage is followed by a classical continuous time comparator stage with output connected to the digital pixel region through logic gates. The pseudo-differential design reduces variation due to mismatch and provides improved rejection of power supply and digital activity noise.

The three analog FEs share the same injection circuit. It allows local generation of analog test pulses starting from 2 defined DC voltages, distributed to all pixels, and a third level, corresponding to a local analog ground. It has been designed to allow two operation modes, which make it possible to generate two consecutive signals of the same polarity or to inject different charges in neighboring pixels at the same time.

3. Chip characterization

In order to characterize the RD53A chip two test systems, BDAQ53 and YARR, have been developed within the collaboration. A large amount of chips (around 300) have been already wire-bonded to Single Chip Cards (SCC) for testing. The characterization of the chip includes X-ray irradiation campaign and test with sensors. The analog and digital operation of the chip has been tested in detail. First tests have shown that the chip works without any major issue and it is possible to correctly configure it. Regarding the analog FEs, the main functionalities have been tested using the S-curve technique. In figure 3 the S-curves taken enabling all the synchronous FE pixels are shown, but similar results have been obtained for the other two designs as well. Figure 4 shows the resulting threshold histogram. Testing with bare chips has shown that the three designs are fully functional and can be operated with stable threshold significantly smaller than 1000 electrons and noise well below 100 electrons, complying with the specifications. X-ray radiation qualification and tests with sensors are ongoing.

4. Final chips implementation

In parallel with the RD53A characterization, the development of the final production chips

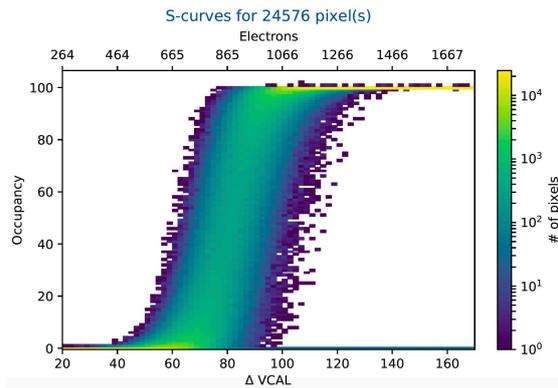


Figure 3: S-curves plot

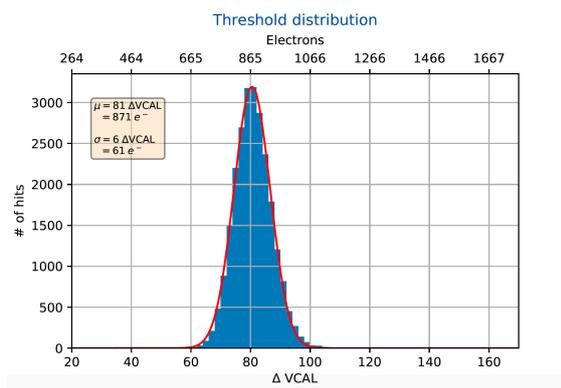


Figure 4: Threshold histogram

has been already started. Two separate chips, one for ATLAS and one for CMS, are envisaged but they will share most of the RD53A-based building blocks. The final chips will contain upgraded versions of building blocks needing improvements together with additional features there were not exploited in RD53A. Among them, a specific biasing scheme for edge pixels and Single-Event-Upset (SEU) hardening will be implemented.

5. Conclusions

The RD53A demonstrator is a large scale prototype intended to be an intermediate step towards the final implementation of the readout chips for the silicon pixel detectors of ATLAS and CMS. An extensive characterization campaign is ongoing. Early results show that the chip works without issues and the all the three analog FEs are showing good results compliant with specifications. In parallel, the development of the final production chip is already ongoing.

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