

The MALTA CMOS pixel detector prototype for the ATLAS Pixel ITk

L. S. Argemi^a, I. A. Asensi^b, I. Berdalovic^c, D. Bortoletto^d, R. Cardella^c, F. Dachs^e, V. Dao^c, T. Hemperek^f, B. Hiti^g, T. Kugathasan^c, K. Moustakas^f, H. Pernegger^c, P. Riedler^c, C. Riegel^h, P. Rymaszewski^f, C. Solans Sanchez^c, E. J. Schioppa^c, A. Sharma^{*c,d}, W. Snoeys^c, C. A. M. Tobon^c, T. Wang^f, N. Wermes^f

^aUniversity of Glasgow, United Kingdom

^bUniversity of Valencia and CSIC (ES), Spain

^cCERN, Switzerland

^dUniversity of Oxford, United Kingdom

^eVienna Institute of Technology (AT), Austria

^fUniversity of Bonn, Germany

^gJozef Stefan Institute, Slovenia

^hBergische Universitaet Wuppertal, Germany

E-mail: Abhishek.Sharma@cern.ch

The ATLAS experiment is planning a major upgrade of its tracking detectors, both strip and pixel, to take full advantage of the High Luminosity LHC. A novel Monolithic Active Pixel Sensor based on 180 nm TowerJazz CMOS imaging technology, dubbed MALTA, has been designed to meet the radiation hardness requirements (1.5×10^{15} 1 MeV n_{eq}/cm^2) of the outer barrel layers of the ITk Pixel detector. MALTA combines low noise ($\text{ENC} < 20 e^-$) and low power operation ($1 \mu\text{W}/\text{pixel}$) with a fast signal response (25 ns bunch crossing) in small pixel size ($36.4 \times 36.4 \mu\text{m}^2$), with a novel high-speed asynchronous readout architecture to cope with the high hit-rates expected at HL-LHC. Extensive lab testing and characterisation in particle beam tests have been conducted on this design and compared with previous prototypes of the same technology. An overview of the sensor technology and readout architecture are presented along with the preliminary results from laboratory tests, radioactive source tests and beam tests.

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*Speaker.

1. Introduction

The ATLAS experiment [1] is one of four major experiments at the Large Hadron Collider (LHC), including CMS, ALICE and LHCb. The LHC will undergo a major upgrade, known as Phase II [2], towards the High Luminosity LHC (HL-LHC) in 2024, to be operational by 2026. The full timeline of the LHC's operation is shown on figure 1. As a result, the ATLAS experiment will also undergo its own upgrade to take full advantage of this increased luminosity. In particular its new Phase II Inner Tracker (ITk) will feature an increased tracking coverage. It will be composed of 4 strip barrel layers and 6 endcap disks for $|\eta| < 2.6$, where η is the pseudo-rapidity $= -\ln(\tan(\theta/2))$, and θ is the angle between a particle and the beam axis. Its Pixel detector will comprise of 5 horizontal barrel layers which may include tilted sensors, to form a closer to normal angle between the interaction point and the sensors towards ends of the barrel layers. The inclined layout option for the ITk Inner Detector is shown on figure 2.

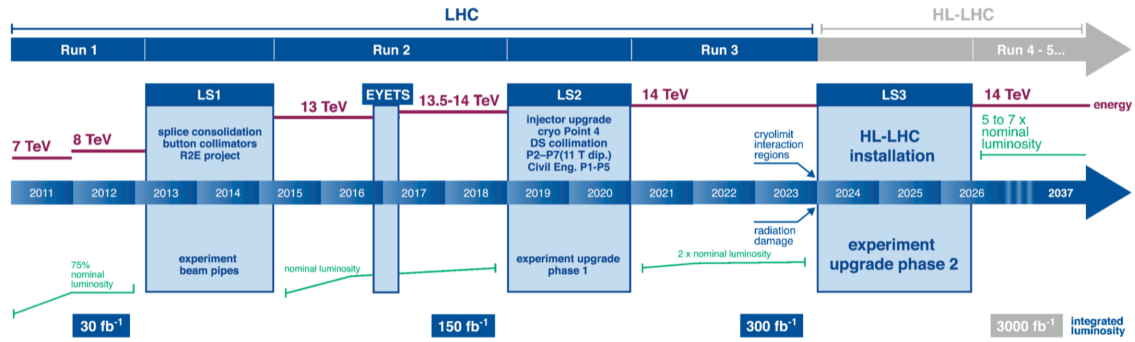


Figure 1: Timeline depicting key milestones in the LHC's development program. [2]

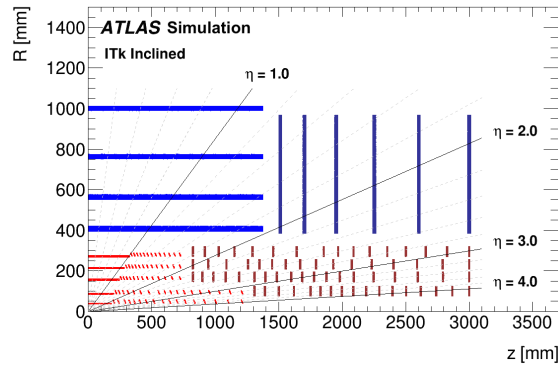


Figure 2: Phase 2 layout of the ATLAS Inner Detector (ITk). Showing in blue the strips and red the pixel layers. [2]

Along with the need for increased radiation hardness, given the expected higher particle hit rates, tabulated on table 1, a substantial effort is also being made to significantly reduce the overall material budget of the detector. The drastic reduction can be seen in figure 3.

This study focuses on the outermost pixel layer, known as layer 4, which is being targeted for being populated by CMOS sensors. Layer 4 would form over 45% of the outer barrel in terms of

Pixel Hit Rate	
Layer	Mhit/mm ² /s
0	27.2
1	8.4
2	1.72
3	1.16
4	0.84

Table 1: Particle hit rates for the various layers of the Phase II Pixel detector.

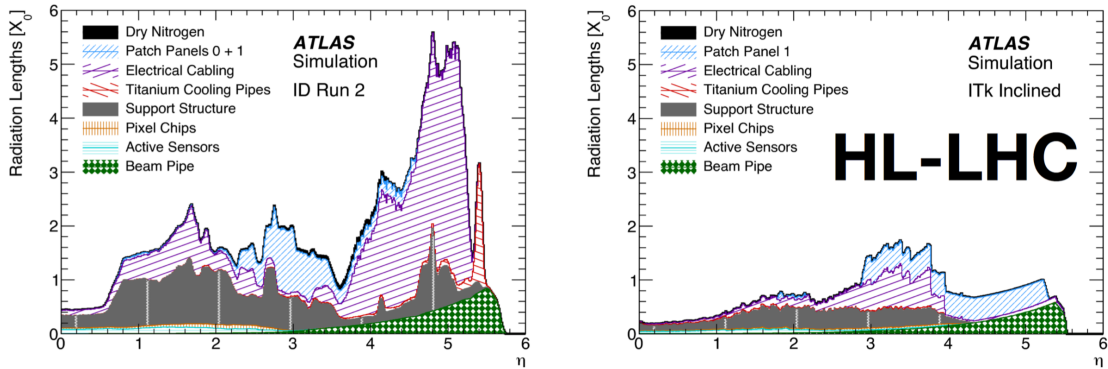


Figure 3: Material budget before the Phase II upgrade (left) as compared to the expected budget for the HL-LHC, shown for various detector components. [2]

module volume. The candidate CMOS sensor is being presented as a drop-in solution to replace the default RD53 hybrid pixel-based modules.

CMOS sensors must achieve a radiation tolerance of $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ for Non-Ionising Energy Loss (NIEL) and 60 Mrad for Total Ionisation Dose (TID). They also must be able to distinguish between hit rates of the order of 100-200 MHz/cm² and reach a timing resolution of 25 ns

2. The TowerJazz MALTA chip

2.1 Technology Reminder

The MALTA [4] sensor is a Monolithic Active Pixel Sensor (MAPS) developed using TowerJazz 180nm CMOS technology inherited from the R&D efforts made towards the ALICE ITS upgrade[3]. It has been designed to have a small collection electrode, of the order of a few square microns, a small input capacitance allowing for a high signal to noise ratio and for a depletion depth of approximately $20 \mu\text{m}$ applied through backside biasing.

To ensure full lateral depletion across the thickness of the sensor, a uniform n-implant in the epitaxial layer has been added. This is referred to as the "modified process" version of the wafer and the cross sections of the original as well as modified process are both shown in figure 4. [5]

There are numerous benefits for the ATLAS experiment in adopting a CMOS sensor option over the typical hybrid solution. This would include the fact that CMOS sensor production is relatively much faster, gaining up to 6 months on schedule. It would also reduce the dependency

on bump bonding. And finally preliminary cost reduction estimates of 50% to 70% are expected as a result.

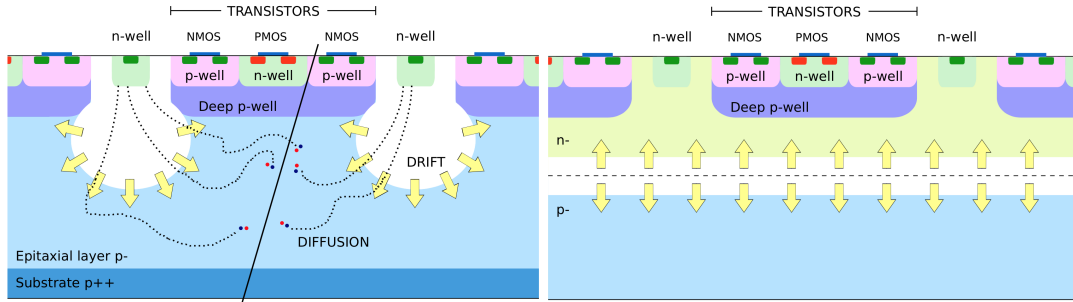


Figure 4: Wafer cross sections of the original process originating from the ALICE ITS [3] sensor (left) as well as the modified process (right), used for the MALTA chip with backside biasing. Not shown to scale.

2.2 Sensor Description

The MALTA [4] sensor, shown in Fig. 5, is a 22 x 20 mm² full size demonstrator comprising of 8 distinct vertical sectors with different pixel flavours. The chip’s matrix architecture is fully clock-less, leading to a low power consumption. Charge deposition information is extracted from the signal’s time walk [7]. Pixel sizes are of 36.4 x 36.4 μm², with the sensor being populated with 512 x 512 pixels in total. Octagonal collection electrodes vary between 2 to 3 μm, reducing the input capacitance, along with differences in the size of the p-well cut-outs around the electrode, described as medium and maximum deep p-well in 5. A separation between this electrode and the nearby electronics of 3.4 to 4 μm is incorporated into the pixel design to minimise cross talk. The power consumption is of the order of 1 μW/pixel for the analogue power (75 mW/cm²) and 10 mW/cm² for the digital power which makes it suitable for layer 4.

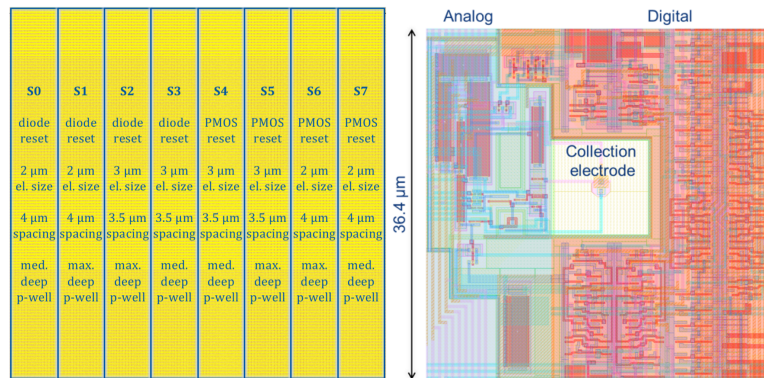


Figure 5: Representation of the 8 different vertical sectors that form the MALTA chip (left) and a close-up view of a single pixel showing the separation between analog and digital circuitry (right).

2.3 Architecture

Groups form individual subsections of 2x8 pixels with pattern assignment to reduce data size from clusters. There are two types of groups. The front-end discriminator output is processed by

a double-column digital logic with the pulse width being adjustable between 0.5 ns and 2 ns. Data are transmitted asynchronously over a high speed bus to the end of the columns without any clock distribution over the active matrix to save power. Two independent buses serve alternating pixel groups (red and blue). There are 22 bits per bus, comprising of the reference (1 bit), the pixel pattern (16 bits) and finally, the group address (5 bits). After passing through the Field Programmable Gate Array (FPGA), additional bits contain the Bunch Cross ID (BCID), the Level 1 Trigger ID (L1ID) and a time of arrival of the signal to the periphery which is proportional to the energy. Each hit is hence represented by a 37 bit word.

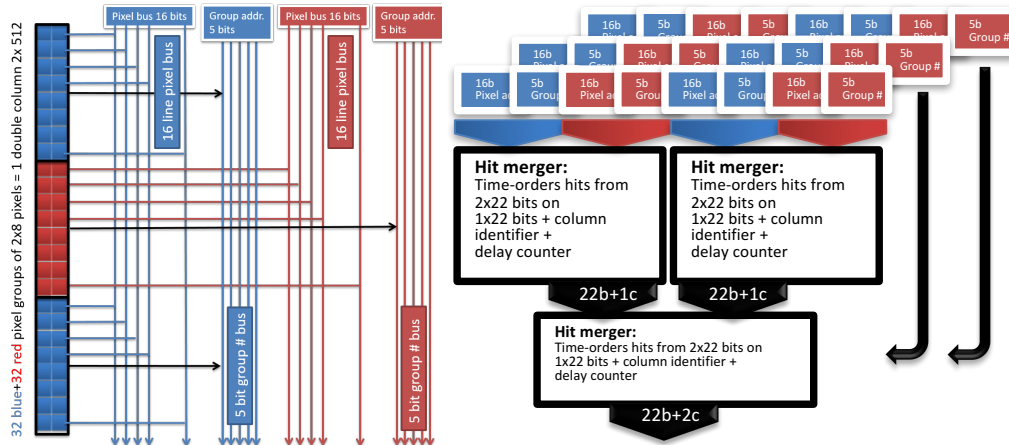


Figure 6: Schematic view of the MALTA double column readout along with the logical sequence at the level of hit merging and arbitration.

2.4 Readout

Every pulse is sampled at a rate of 4 Gbps. For a 1 ns pulse, the time resolution is of the order of 390 ps, where 37 individual signals are sampled. The spread between these readings is of under 1 ns and an efficiency greater than 99%. No temperature dependence (between 10 to 40°C) has been observed. Temporal corrections of the order of 250 ps, known as taps, for each of the 37 signals are applied in order to align the rising edge of each signal. A tap calibration measurement result is shown on figure 7, where 300 pulses (each 2 ns long) are propagated along all 37 signal lines and their time of arrival is correspondingly adjusted using taps for a synchronised readout.

3. Laboratory Measurements

All samples discussed in the subsequent sections implement the modified process detailed in section 2.1. As this document describes ongoing characterisation efforts, chip configurations are not always identical as they undergo iterative improvements in DAC parameter settings. This can have the result of shifting the threshold values displayed on some of the subsequent plots presented. MALTA comprises of 8 analogue monitoring pixels. These bypass the digital circuitry altogether and provide a direct access to the analogue output. This makes it possible to perform timing as well as gain measurements using radioactive sources. One such source made use of is ^{55}Fe , through which figure 8 was produced. The timing measurements reveal that the charge collection

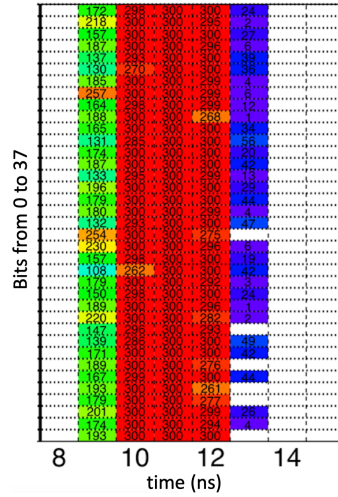


Figure 7: Synchronised readout of 37 signal lines reading 300 pulses each, where the pulse duration is of 2 ns, with applied taps adjusting the time of arrival accordingly.

time and front-end timing are overwhelmingly within the 25 ns requirement. The energy resolution performance shows some degradation after proton irradiation to the 10^{15} n_{eq} , but still allows for the observation of the two distinct $k\text{-}\alpha$ and $k\text{-}\beta$ peaks produced by the ^{55}Fe source, known to be equivalent to 5.19 keV and 6.49 keV, respectively.

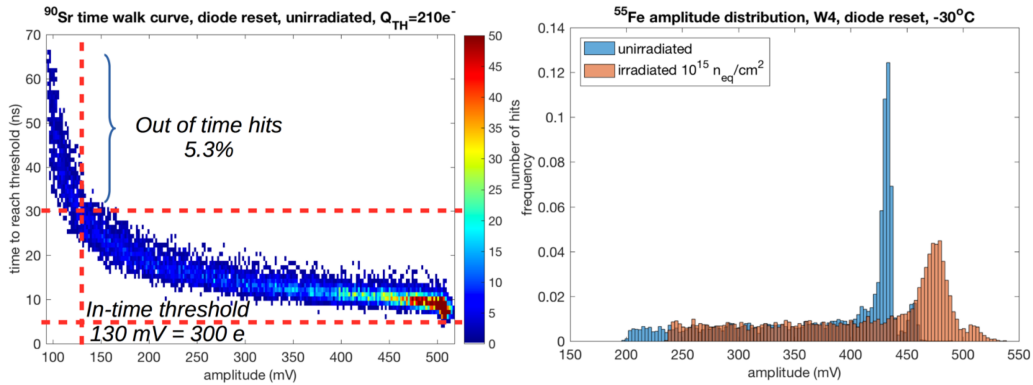


Figure 8: ^{55}Fe source measurements, showing timing results (left) and energy resolution performance of the sensor (right).

Similarly, the gain can be estimated from the amplitude difference between these $k\text{-}\alpha$ and $k\text{-}\beta$ peaks. This is performed by obtaining the ratio of the amplitude difference between both peaks and the difference between the $k\text{-}\alpha$ and $k\text{-}\beta$ energies. The variations in these values as a function of substrate voltage are tabulated in table 2.

Another characterisation parameter assessed for this sensor is the threshold dispersion. This involves pulsing a pixel by injecting charge of varying magnitude a given number of times. By pulsing pixels in this manner, the absolute value of the threshold for each pulsed pixel can be obtained by the point at which the pixel fires half of the time. The behaviour is a turn-on curve (or S-curve). Such an S-curve is shown on figure 10. Repeating this process for a large number of pixels provides a distribution, or dispersion, of the thresholds across the pixel sample. The

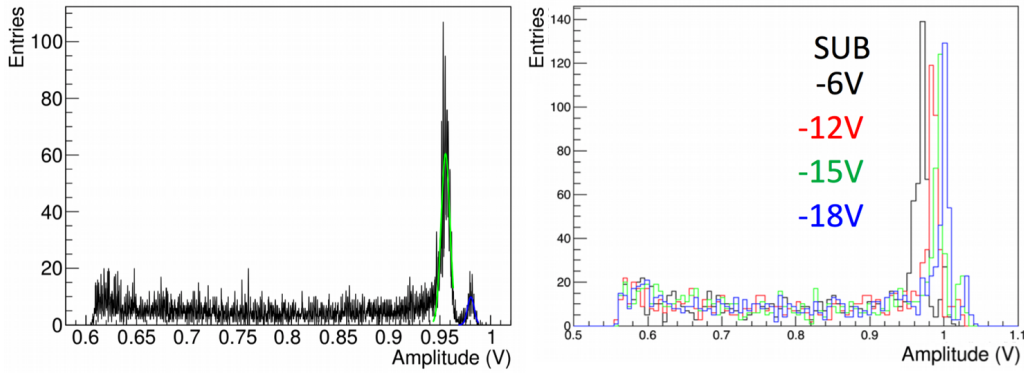


Figure 9: Gain measurements performed using an ^{55}Fe source. The full spectrum of the energy response (left) has fits applied to the $k\text{-}\alpha$ and $k\text{-}\beta$ peaks in order to extract their mean amplitude value. The variation in the amplitude difference between both peaks as a function of the substrate voltage is shown on the right.

Pixel Hit Rate	
SUB (V)	Gain \pm 0.002 (mV/e)
-6	0.1464
-12	0.1480
-15	0.1371
-18	0.1364

Table 2: Gain measurements on an unirradiated MALTA sensor obtained using its response to ^{55}Fe for varying substrate voltages.

threshold dispersion is yet another parameter of the specifications for the layer 4 CMOS candidate sensors. In the case of the MALTA sensor, this threshold dispersion was measured to be twice as large as the intended design, with a width of just over 40 electrons.

Threshold dispersion measurements were repeated on a 70 Mrad X-ray irradiated sample, which yielded a 50% increase in its width. The noise, obtained by the slope of the threshold measurement S-curves (where a steeper slope would correspond to a lower noise level), are also observed to increase post X-ray irradiation. Figure 11 summarises these results.

It can be seen that analogue circuits are TID sensitive, especially when current levels are very small and comparable potentially to radiation induced leakage currents. Nevertheless, the circuit was observed to be functional after after a TID level of 70 Mrad.

4. Test-beam measurements

A test-beam campaign was conducted on the MALTA chip at CERN's Super Proton Synchrotron (SPS) facility providing 180 GeV/c pions. The telescope assembly, named KARTEL [6], used to gather the necessary track reconstruction data comprised of 6 MIMOSA planes with a overall resolution of under $2\ \mu\text{m}$ [6]. Irradiated samples were kept cold by a silicon-oil refrigeration system at -20°C and the samples tested included unirradiated, $5 \times 10^{14} n_{eq}/\text{cm}^2$, neutron irradiated $1 \times 10^{15} n_{eq}/\text{cm}^2$ and X-ray irradiated 80 Mrad.

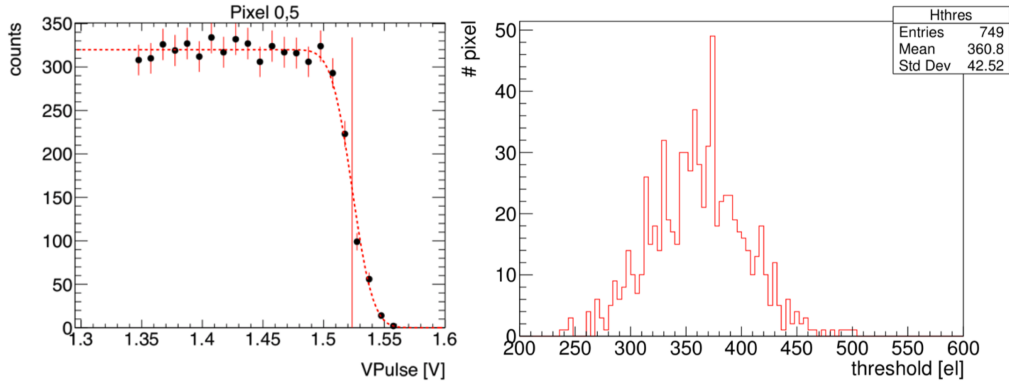


Figure 10: S-curve produced by pulsing pixels multiple times at varying threshold levels (left) along with the distribution of thresholds for over 700 pulsed pixels (right), showing a distribution width of just over 40 electrons.

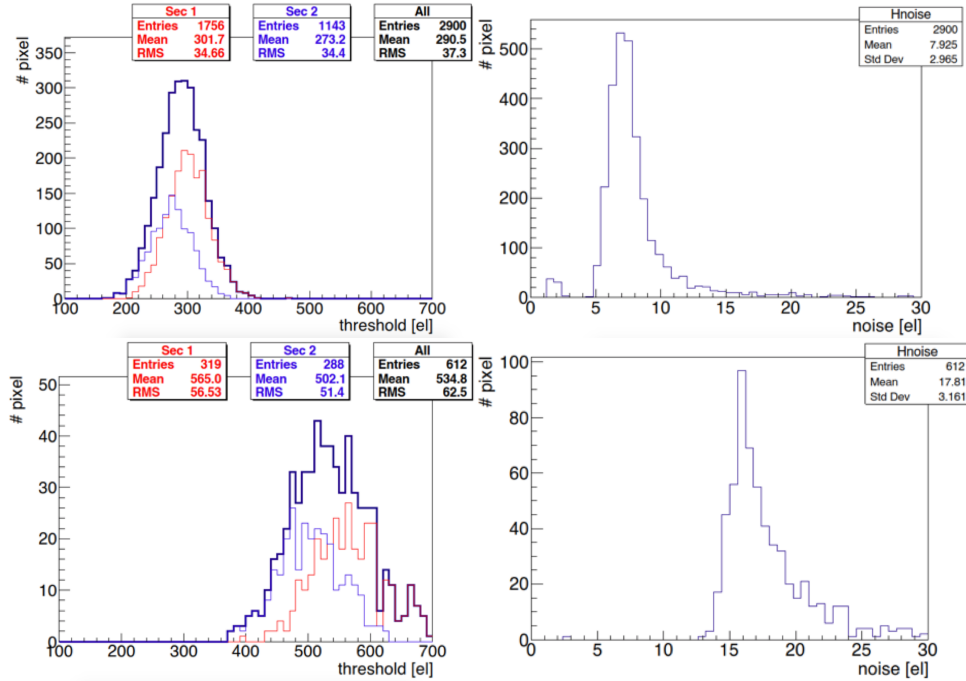


Figure 11: Threshold dispersion measurement showing unirradiated sample data (left), X-ray irradiated sample data (right) with the top row displaying the increase in threshold dispersion by over 50% after 70 Mrad of irradiation. The bottom row shows the corresponding increased noise effect post irradiation. Threshold dispersions are shown for MALTA sectors 1 and 2 as described in 2.2.

The cluster size, or number of surrounding pixels that register a hit upon a particle track traversing the MALTA sensor can be obtained through track reconstruction conducted using the purpose built Proteus framework [6]. The cluster size measurement was assessed for varying thresholds for both unirradiated as well as neutron irradiated ($5 \times 10^{14} n_{eq}/cm^2$) chips. Figure 12 compares the cluster size for sector 4 of the unirradiated sample for decreasing threshold levels. A clear increase in the cluster size can be seen when the threshold is decreased from ~ 600 to ~ 250 electrons, as would be expected.

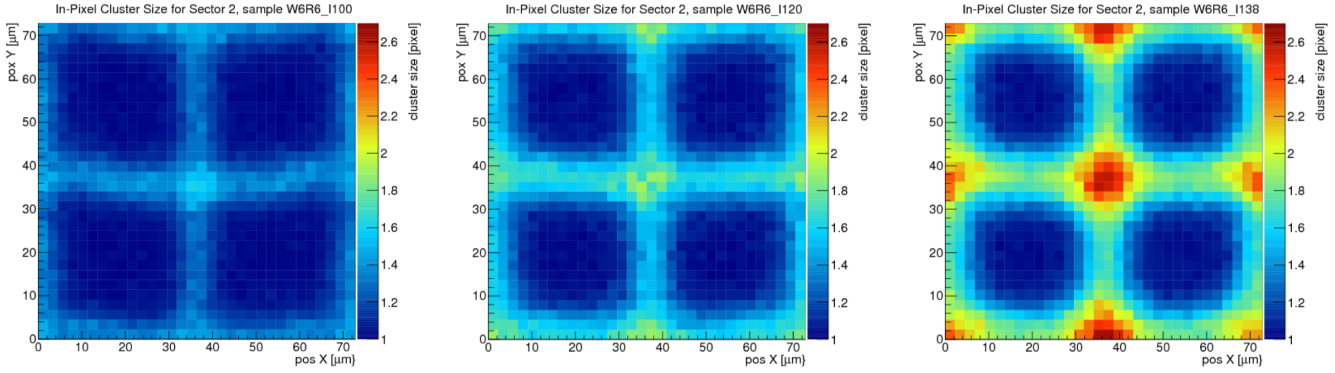


Figure 12: Variation in cluster size for an unirradiated MALTA sample at decreasing thresholds (from ~ 600 to ~ 250 electrons).

Given the high resolution of $2 \mu\text{m}$ of the telescope, in-pixel efficiency could also be probed. This is shown on figure 13 where the corners of the pixels are revealed to be low efficiency regions.

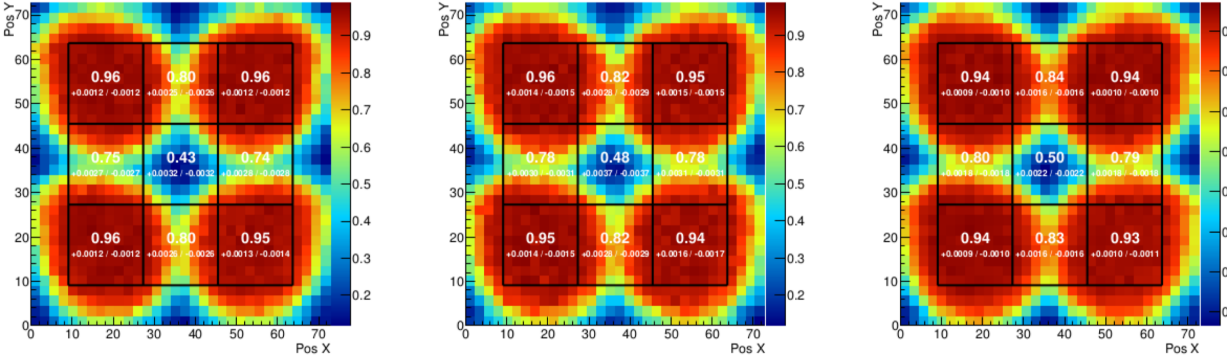


Figure 13: In-pixel efficiency on a neutron irradiated $1 \times 10^{15} n_{eq}/\text{cm}^2$ sample at decreasing thresholds (~ 600 to ~ 250 electrons), showing an increase in inter-pixel efficiency as well as decrease pixel center efficiency. No time cuts are applied to these efficiency measurements.

Though the efficiency at the center of the pixel is expected to increase with decreasing threshold, the opposite effect is observed in these samples. This efficiency reduction at the pixel center arises partly due to issues at the masking and merging level. Additionally the pixel centres have a higher probability of collecting the total charge (above threshold) from an energy deposition leading to these regions being more sensitive to noise hits. Similarly, inter-pixel regions have lesser sensitivity to noise hits as the likelihood is greater that the charge deposited between pixels will be collected by two or more pixels, reducing the chances of a noise hit causing the pixel hit to be classified as a fake it. This behaviour is observed consistently across all samples.

The shape of the p-well extension has an effect on the contour of the efficiency as seen in figure 14 where sector 3 incorporates the so called "medium deep p-well" and sector 4 the "maximum deep p-well". Their respective layer cut-outs are also shown. This difference between p-well shapes becomes increasingly visible on irradiated chips at high threshold.

Figure 15 summarises the efficiency trends drawn from the test-beam campaigns.

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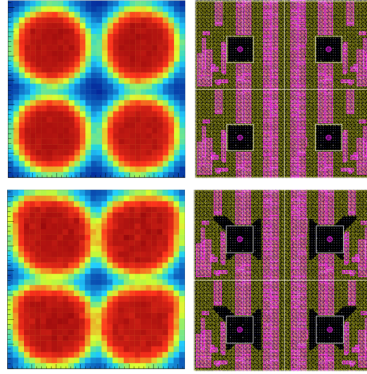


Figure 14: A qualitative view of the effect of the p-well cut-out shape on the subsequent contours of the pixel efficiency maps.

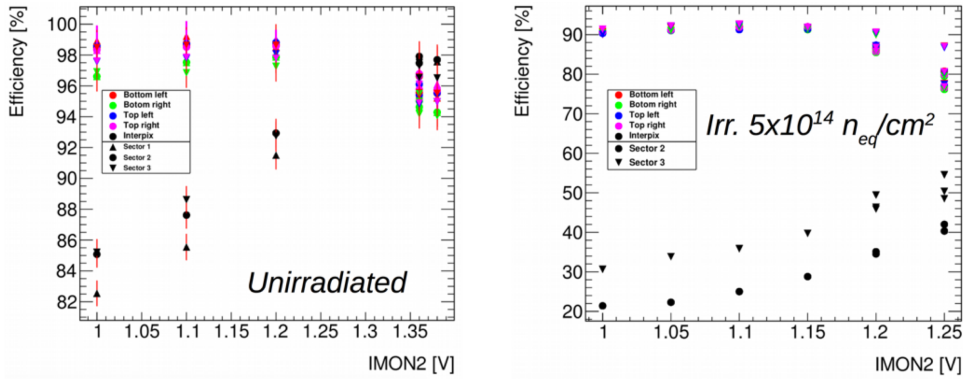


Figure 15: Left: Efficiency variation as a function of threshold set by the DAC parameter IMON2 for an unirradiated MALTA sample, where the pixel centre efficiencies reduce with lower threshold (higher values of IMON2) and conversely where the inter-pixel efficiency increases, as expected, with lower thresholds. Right: Post $5 \times 10^{14} n_{eq}/cm^2$ neutron irradiation, a substantial efficiency loss can be observed at the inter-pixel region, whilst simultaneously retaining $>97\%$ efficiency at most thresholds at the pixel centers. The in-time efficiency was observed to be $> 90\%$.

5. Conclusions

The MALTA sensor is a full demonstrator monolithic CMOS sensor produced in 180nm TowerJazz technology. It uses a novel asynchronous readout with no clock being distributed over the matrix to minimize power consumption. Its design integrates a small charge collection electrode for low capacitance and low analogue power consumption. Measurements have been performed on unirradiated and neutron irradiated samples ($5 \times 10^{14} n_{eq}/cm^2$ and $1 \times 10^{15} n_{eq}/cm^2$). This led to the observation that as the merging logic is forced off it causes some hits to be lost due to erroneous merging of those true hits with noise hits.

Analogue tests showed over 95% of hits being registered within the 25 ns in-time efficiency requirement. This was also measured at low noise levels.

Most issues observed in the test-beam results are explained by the degraded detection efficiency, especially in the pixel corners due to masking and merging errors, the higher than expected threshold spread as compared to simulations. The next design submission of the chip will hence

also include adjustment bits for greater threshold settings control.

All other issues that have been identified through this study will be addressed in the next iteration of the sensor design with very promising performance for the phase II upgrade of ATLAS.

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References

- [1] *The ATLAS Collaboration, The ATLAS Experiment at the CERN Large Hadron Collider, JINST 3 (2008) S08003.*
- [2] *ATLAS Collaboration, Technical Design Report for the ATLAS ITk Pixel Detector, Tech. Rep.*
- [3] *L. Musa, CERN-LHCC-2013-024; ALICE-TDR-017.*
- [4] *H. Pernegger et al., First tests of a novel radiation hard CMOS sensor process for Depleted Monolithic Active Pixel Sensors, JINST 12 (2017) P06008.*
- [5] *W. Snoeys et al., A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance, NIM A 871 (2017) 90 – 96.*
- [6] *G. McGoldrick, M. Cerv and A. Gorišek, Synchronized analysis of testbeam data with the Judith software, NIM A 765 (2014) 140 – 145.*
- [7] *I. Berdalovic et al., Monolithic pixel development in TowerJazz 180 nm CMOS for the outer pixel layers in the ATLAS experiment, JINST 13 (2018) C01023*