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# Pixel detector for CMS upgrade

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The LHC machine upgrade program will increase the instantaneous luminosity delivered to the multi-purpose experiments up to 7.5x$10^{34}$ $cm^{-2}s^{-1}$ in 2026, with the goal of an integrated luminosity of 3000 $fb^{-1}$ by the end of 2037. In order to fully exploit this luminosity, CMS plans to build a completely new pixel detector. The Phase-2 pixel detector relies on highly radiation tolerant sensors and a new ASIC based on 65 nm CMOS technology. A high bandwidth readout system and a novel serial powering scheme of the pixel modules will be used to accommodate the highly demanding system needs. These prospective design choices as well as new layout geometries with acceptance extended from $|\eta| < 2.4$ to $|\eta| < 4$, will be presented along with some highlights of the R&D activities.

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## 1. Introduction

After the end of the Long-Shutdown 3, the LHC will enter its High-Luminosity phase (HL-LHC), reaching 5 to 7 times its nominal luminosity. Starting from 2026, the instantaneous luminosity delivered to the experiments will be increased up to 7.5x10$^{34}$ cm$^{-2}$s$^{-1}$, aiming to an integrated luminosity of 3000 fb$^{-1}$ by the end of ten years of operation. The increased instantaneous luminosity corresponds to an increased number of interactions per bunch-crossing, or pile-up, to 140-200, leading to high values of occupancy and unprecedented levels of radiation up to 1.2 Grad [1]. In preparation for the HL-LHC, the CMS experiment will be also undergoing a major upgrade, known as Phase-2ful Upgrade, to be able to be fully functional and highly performant in the new HL-LHC environment.

In particular, a completely new all-silicon CMS Tracker will be built to achieve the required physics performance [2]. The HL-LHC operating conditions pose significant challenges for the design of the innermost part of the detector, the Inner Tracker (IT). The most significant challenges and design choices to face them are listed below:

- Extended acceptance of the IT system is achieved by a new layout, shown in Fig. 1 (left), covering the forward pseudorapidity up to $|\ \eta\ | = 4$ for efficient mitigation of the pileup and improvement of the vertex reconstruction efficiency. More details on the detector layout are presented in Sec. 2.1.

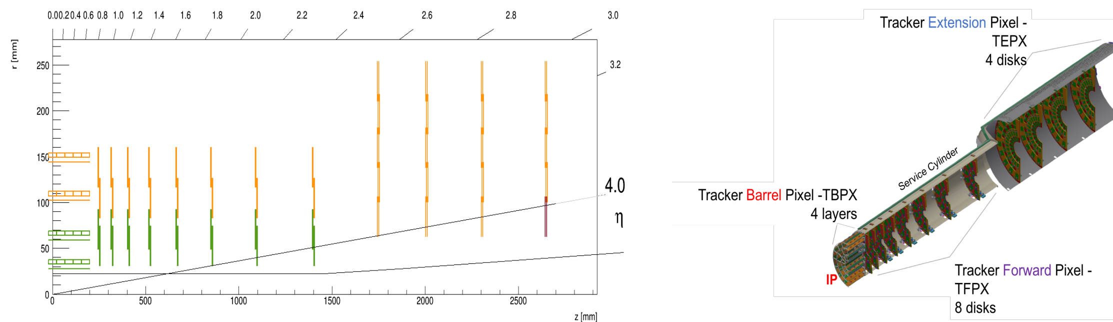


**Figure 1:** (Left) New proposed layout extending up to $|\eta| = 4$. (Right) A quarter of the CMS IT system.

- Enhanced radiation tolerance is required to maintain robust tracking performance. The innermost layer of the IT will be exposed to a total ionising dose of 1.2 Grad and 2.3e16 n.eq./ cm$^2$. An intensive R&D effort is ongoing for the development of sensors and the readout chip that will operate without degradation in functionality throughout the lifetime of the detector, presented in Sec. 3.1 and 3.2, respectively. Furthermore, the IT system is designed, such that it is easily extractable during shutdowns for maintenance and potential replacement of the deteriorated parts.

- A reduced material budget is important to ensure robust tracking performance: the Inner Tracker is the main pattern recognition device for track reconstruction in CMS, and material inside the Inner Tracker volume affects track finding efficiency and fake rate due to hadronic interactions and multiple scattering; in addition, the precision in the track parameters' estimation is also affected. Novel techniques have been developed for a design of a

light-weight detector. The pixel modules will be powered with a new serial powering scheme (see Sec. 3.3), readout by low-mass fast electrical links (see Sec. 3.4), mounted on carbon-fibre structures and cooled by CO2 evaporative cooling. These design choices will allow for minimisation of the material for the services and the mechanics (see Sec. 2.3).

- Higher granularity is required to maintain adequate occupancy of less than 0.1% and robust track separation. The CMS IT system will be composed of 2 billion pixels of 2500 $\mathrm{um}^2$ each. A small-pitch pixel readout chip is designed in 65 nm CMOS technology and has to cope with extreme hit rates of up to 3.2 GHz/ $\mathrm{cm}^2$, an increased trigger rate of 750 kHz and 12.5 us trigger latency leading to higher readout rates and hit buffering requirements. The highly performant readout chip is complemented by a high-bandwidth readout system composed of fast and light electrical links, optoelectronic boards and optical links and a new data acquisition back-end board, presented in Sec. 3.4, 3.5, 3.6.

## 2. Key design choices

### 2.1 Layout

The CMS IT System will cover a total surface of 4.9 $\mathrm{m}^2$ with 3892 hybrid modules. A quarter of the IT is shown in Fig. 1 (right). It is composed of a barrel part (TBPX) with four cylindrical layers (L1, L2, L3, L4), a forward part (TFPX) with eight small disks per end and an extension part (TEPX) with four larger disks per end. For the optimisation of the module production, only two types of modules are used; double-chip (1x2 chip) modules for the inner layers and ring and quad-chip (2x2 chip) modules for the outer ones, shown in green and orange in Fig. 1 (left). The barrel, forward and extension will be mounted in half-cylinders that will hold their services. There will be no mixing of service among the four half-cylinders, in each of the three subsystems.

The inner layer is exposed to the most harsh environment, sitting only 30 mm from the beam. In case sufficient radiation tolerance is not achievable for the whole detector lifetime, this part of the detector could be replaced after 5 years of operation. The TBPX pixel modules are arranged in ladders. Each ladder is split in z into two parts, one long (5 modules) and one short (4 modules), the short and long ladders are interleaved among the layers and will be complemented by the other z-end, such that there is no projective gap at $|\eta| = 0$, as shown in Fig. 2 (left).

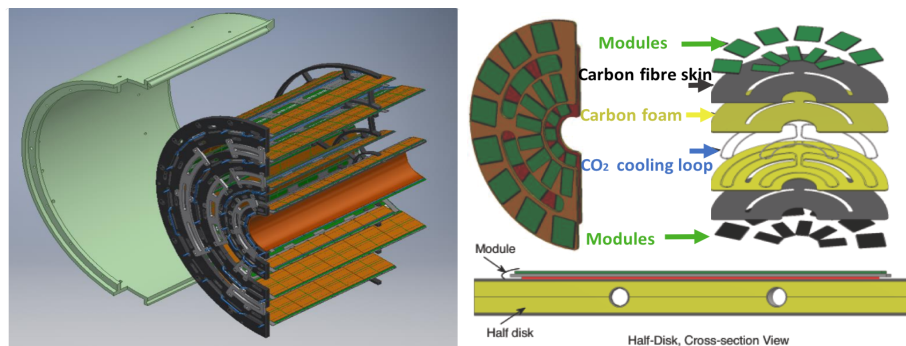


**Figure 2:** (Left) CAD drawing a quarter of TBPX. (Right) Sketches showing details of TFPX dee structures.



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The TFPX and the TEPX are arranged in concentric rings (4 for TFPX, 5 for TEPX) with modules overlapping in both in r and r-$\phi$, ensuring hermetic coverage. Each TFPX disk is physically made out of two half-disks; one that supports the odd rings and one that supports the even rings. Each of these disks are split in half into D-shaped structures known as "Dees" (see Fig. 2 (right)), where modules are arranged on both sides of a "Dee"-sandwich structure. The TEPX disk design will follow the same rationale of double-disks. It is currently considered to use the inner ring of the last disk of the TEPX, shown in red in Fig. 1 (left), which is below the $|\eta| = 4$ acceptance as a dedicated luminosity and background monitor with independent operation to the rest of the system. In addition to this, an extra 10% of triggers (75 kHz), tagged as lumi-triggers, will be provided to all four disks of the TEPX for the measurement of the online bunch-by-bunch luminosity and background. These triggers will be distributed along the orbit and will acquire data that will be analysed separately by the back-end electronics.

### 2.2 Modules

The pixel module design is based on the hybrid technology, i.e. pixel sensors bump-bonded to pixel chips wire-bonded to High-Density Interconnects (HDI). The HDIs are used to distribute signals and power to and from the pixel modules. The design of the pixel modules is simple and robust, with the pixel readout chip being the only active component and no other auxiliary electronics used. Only a few passive components, mostly decoupling capacitors and connectors are hosted on the HDI. Each module will have dedicated readout links and a serial power connection is used among adjacent modules such that the current of one module "feeds" the other. Prototype HDIs have been designed in 2018 to readout modules with the prototype readout chip (RD53A [4]), as shown in Fig. 3 (left). The first two prototypes powered in a serial power chain and readout by an adapter board is shown on Fig. 3 (right).

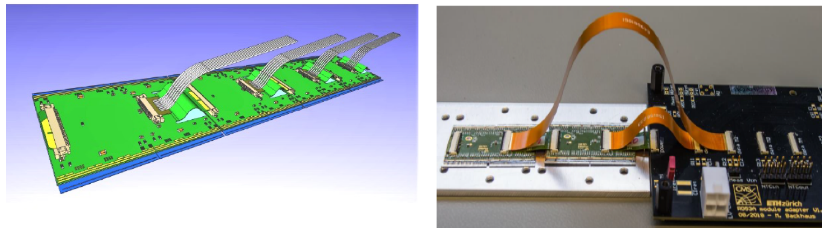

**Figure 3:** (Left) A serial power chain of four barrel modules readout by dedicated readout links. (Right) Two prototype 2x2 HDIs for RD53A chip powered in series and readout by an auxiliary readout board.

### 2.3 Mechanics

The CMS IT design is based on simple mechanical structures to support the modules and the services made of low mass carbon foam/fibre. The first "Dee" structure and a prototype of the service cylinder were fabricated in 2018 and are shown Fig. 4 (right). A highly performant cooling system has been chosen based on bi-phase $CO_2$ coolant, which also allows for minimisation of the pipe material. The high performance of the IT cooling is essential not only for the sensors, but also

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for the longevity of the readout chip[1]. In Fig. 4 (left), a barrel cooling loop shows how a cooling pipe will be used to serve two adjacent ladders.

**Figure 4:** (Left) A cooling loop serving the inner barrel layer routed right below the bottom of the chip hotspots. (Right) The first samples of the TFPX Dee's structures and the service cylinder built in 2018.

## 3. Novel Technologies

### 3.1 Sensors R&D

An intensive ongoing R&D effort is dedicated to the development of radiation-hard, small-pitch sensors. The arrival of the radiation hard, prototype readout chip (RD53A) allowed to test modules in test-beams after irradiating them up to $1e^{16}$ n.eq./ $cm^2$. Special light-carrier boards have been designed in 2018 to minimise the amount of material behind the chip and enable easy handling of irradiated modules(Fig. 5 (left)).

Planar n-in-p sensors are considered as baseline with optimised thickness around 100-150 um in order to be more radiation tolerant without compromising the amount of collected charge. The n-in-p sensors can have significant voltages near the grounded chip, causing a danger of sparking, therefore a spark protection needs to be developed and tested in 2019. The thin n-in-p sensors may not be able to handle the expected integrated radiation dose in the innermost layers of the detector, therefore 3D sensors are also being considered. Since the distance between electrodes is significantly smaller, being vertical, the radiation tolerance is increased. Nevertheless, the 3D sensors option is considered only for the innermost layers due to their complex fabrication and higher cost.

Beam tests carried out in 2018 have given very promising first results for both planar and 3D sensors [3]. A preliminary result from a planar sensor irradiated to the radiation levels of TBPX L3, tested at a test-beam at DESY is shown in Fig. 5 (centre). Rectangular cells of 25x100 $um^2$ have so far been considered as baseline, but significant cross-talk has been measured between adjacent pixels on single-chip modules with rectangular cells. More studies are needed to conclude on the optimal system choice (Fig. 5 (right)).

### 3.2 RD53 Pixel Readout Chip

The pixel readout chip is being developed by the RD53 collaboration, which is a common effort, shared between ATLAS and CMS inner tracker systems. The goal of this collaboration is

[1]Radiation damage in the 65 nm CMOS technology is mitigated when the radiation is received at low temperature.



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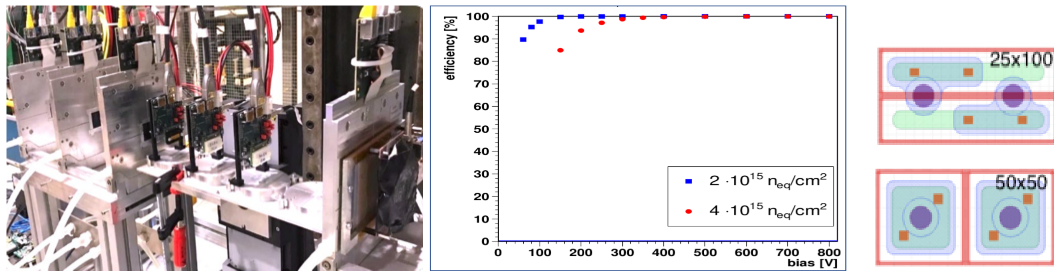


**Figure 5:** (Left) Three modules mounted on light-carrier boards in a test-beam in 2018. (Centre) Test-beam result from a thin planar sensor showing efficiency levels of >99% after irradiation with sufficient bias voltage provided. (Right) Example designs of rectangular (25x100 um$^2$) and square(50x50 um$^2$) pixels showing n+ implants (green), metal layers (blue), p-stop (red), contacts (orange), bump-bond pads (purple).

the development of designs and methods for a hybrid pixel detector readout chip in a 65 nm CMOS technology. The RD53A chip, the first large scale demonstrator, was produced in 2017 and became available to users in 2018. It has approximately half the size of the final chip, and it contains architecture variations for testing purposes, namely three design variations of Analog Front Ends (AFE) and two digital readout architectures, which explore two approaches on buffering resources shared in a limited pixel area. The pixel matrix is made of 192x400 pixels with a pixel size of 50x50 um$^2$ with analog islands (manual layout) being placed in a digital sea (synthesised). The chip periphery located at the bottom of the chip contains digital and analog circuitry needed to bias, configure and monitor the functionality of the chip. It includes two Shunt-Low Dropout (Shunt-LDO) regulators that enable the serial powering of the pixel modules distributed along the bottom of the chip for thermal management and reliability reasons, four fast (1.28 Gbps) data output links using the Aurora protocol and a control link (160 Mbps), as shown in Fig. 6 (left).

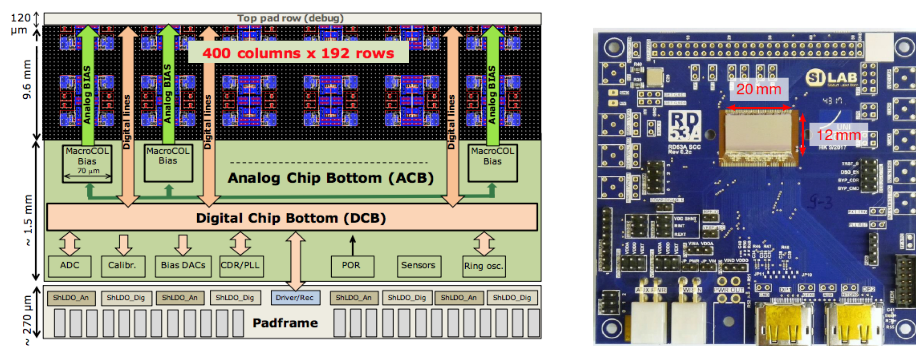


**Figure 6:** (Left) Functional floorplan of the RD53A chip with the main blocks. (Right) A Single Chip Carrier (SCC) developed for testing the RD53A chip.

The RD53A chip has been tested extensively during 2018 using a test board that was developed by the RD53 collaboration (see Fig. 6 (right)). The chip has been proven to be fully functional, meeting the 500 Mrad tolerance specification. All AFE variants have demonstrated good performance with radiation and have achieved a low operational threshold of $\sim$1 ke-. A threshold distribution of one of the AFE is shown in Fig. 7 [5]. The AFE choice that will be integrated in



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the final CMS chip is expected in early 2019, based on results from ongoing extensive tests of the three AFE variants and Monte Carlo simulations to evaluate the expected tracking performance. The RD53 design team has already started working on the RD53B design aiming at the CMS final chip submission by the end of 2019.

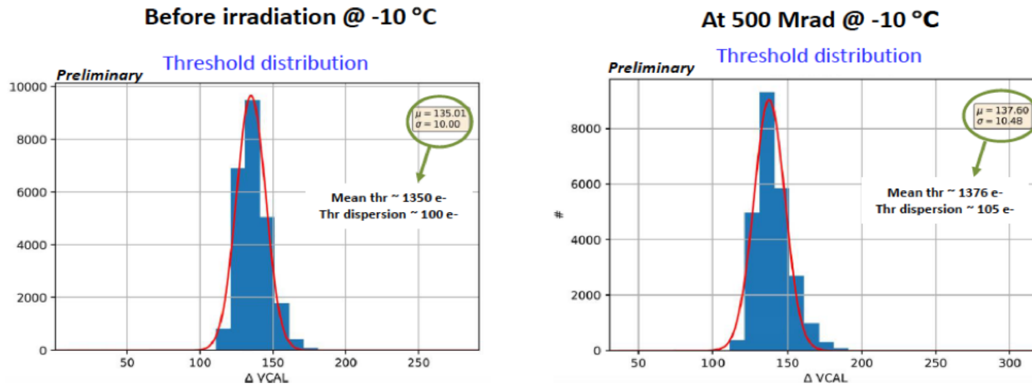


**Figure 7:** A threshold distribution before and after irradiation to 500 Mrad for one of the RD53A AFE variants ("Linear Front-End").

### 3.3 Serial Powering

The specifications for the future readout pixel chip impose the use of sub-micron CMOS technology, featuring low voltage supply to guarantee the target resolution and a sustainable power density while still implementing all the required functionalities. Each pixel chip will consume about 2 A and both analog and digital domains will be powered with 1.2 V. The use of DC-DC power conversion has been excluded due to radiation hardness and material budget reasons. Therefore, a serial power distribution system has been proposed.

This scheme is a novel solution never attempted in a large-scale detector and it fulfils the requirements of high current power distribution with acceptable power cable losses, radiation tolerance and adequate material budget. The implementation is based on Shunt-LDO regulators integrated on the bottom of the chip. Two independent Shunt-LDO regulators [6], powered in parallel, provide independently the analog and digital supply voltages to the chip core with configurable input impedance (slope) and offset for optimal power dissipation and current sharing, as shown in Fig. 8 (left). These regulators require a minimum 200 mV drop-out voltage for stable operation i.e. a minimum input voltage of 1.4 V has to be provided to the chip, such that the Shunt-LDO regulators can provide 1.2 V to the analog and digital domains. Any extra injected current not consumed by the chip will be shunted at the bottom of the chip, creating a hotspot. Therefore, the cooling pipes should be routed close to the periphery of the chip. The power consumption of the chip at maximum hit and trigger rates, including any Shunt-LDO losses, is expected to be $< 1\ \mathrm{W/cm^2}$.

Serial power loops feed the required supply current to chains of 5-11 pixel modules, with the two or four pixel chips on each module connected in parallel. The maximum number of modules in a chain is set to 11 modules, resulting to a total of $\sim$530 serial power chains needed to power 4k pixel modules. In 2018, system tests were performed demonstrating the successful operation of serial power chains using 8 single RD53A modules and 8 RD53A bare chips. The setup is depicted

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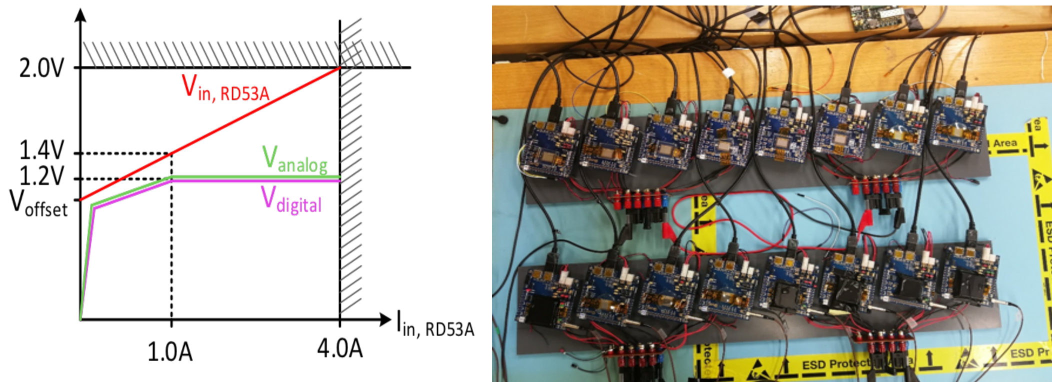


**Figure 8:** (Left) Voltage vs. current behavior of the RD53A chip load model, showing the output voltages used to power the digital and analog power domains and the configurable slope and offset for the input voltage. (Right) System test of 16 RD53A chips and modules used to optimise the operation of the serial powering system.

in Fig. 8 (right). The system has been proven very robust and the Shunt-LDO is very reliable and radiation tolerant. The high-voltage distribution of the system will be following the granularity of the serial power chains for the planar modules. The high-voltage distribution scheme for the chains powering 3D sensor modules will be different, i.e. more granular, to avoid accidentally biasing the sensors due to the voltage drops that appear along a chain.

### 3.4 Low-mass electrical links

High-speed electrical links (e-links) will be deployed to achieve the bandwidth needed to exploit the increasing luminosity and to allow data acquisition at higher rates. The data readout links will be running at 1.28 Gbps with Aurora protocol, while the control links will be running at 160 Mbps with a custom-made protocol. These e-links have to be as short and light as possible (maximum length of ∼1 m) and will connect the pixel modules to opto-boards. Both flat flex and twisted pair options are being currently explored, shown in Fig. 9 (left). These electrical links need to be AC-coupled, since the modules' "local" grounds along the chain differ due to serial powering. Special protocols with DC-balanced symbols, such as Aurora, have been chosen for this reason and are combined with decoupling capacitors close to the receiver side.

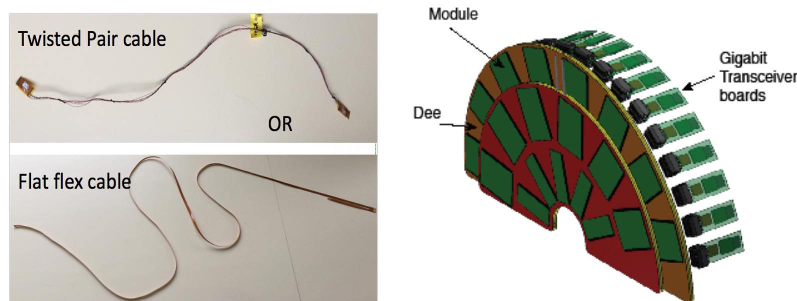


**Figure 9:** (Left) E-links samples tested in 2018. (Right) Opto-boards located at the periphery of the disks.



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This comes a bit as a surprise. I think you should first mention that the chip has data aggregation capability, enabling the possibility to implement multiple links per chip or aggregating 2 or 4 chips of a module into a single link, so that the density of e-links can be adapted to the data rates in the different parts of the detector.

Each Low-Power GigaBitTransceiver (LpGBT) [7] chip supports up to 7 readout links at 1.28 Gbps and 8 control links at 160 Mbps. An efficient data formatting provides a reduction of the data volume by about a factor of two, compared to a simple scheme where each pixel hit would be encoded with its full address. The chip will have data aggregation capability, enabling the possibility to implement multiple links per chip or aggregating 2 or 4 chips of a module into a single link, so that the density of e-links can be adapted to the data rates in the different parts of the detector. In the current layout, a maximum number of 6 links per module is used in the innermost barrel layer, whereas one single link is sufficient to readout a quad-chip module in the outer regions of the detector.

One control link per module is used. For the entire IT system, 10800 electrical links will be used to readout and control 3892 pixel modules with 778 opto-boards. Two rules have been followed on the design of the connectivity of the system: i) an opto-board cannot readout modules belonging to different serial power chains to avoid mixing reference grounds, ii) a module cannot be readout by more than one LpGBT, to avoid synchronisation problems among multiple LpGBTs.

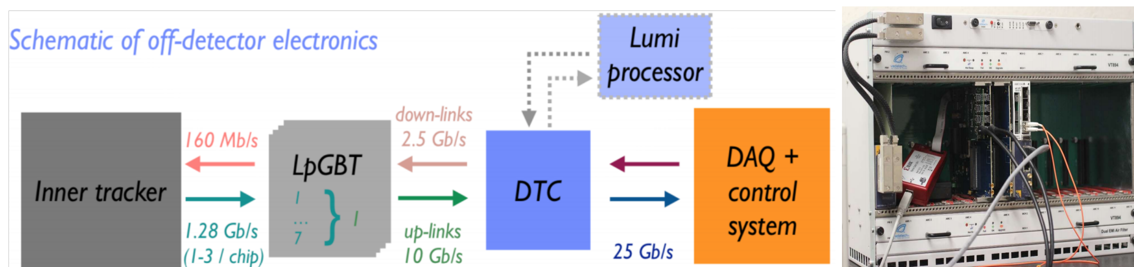


**Figure 10:** (Left) The path of the data and the controls from the pixel modules to the DAQ. (Right) A uTCA crate hosting a uDTC with a mezzanine card that can readout multiple RD53A modules.

### 3.5 Opto-boards

The next step of the readout data is the conversion to optical links at 10 Gbps done by the opto-boards, which host the LpGBTs and the Versatile Links (VL+) [8]. An opto-board is powered by a pair of DC-DC converters, which provide power to two LpGBTs and two VL+. The opto-boards cannot be placed on the pixel modules due to their radiation tolerance, which is limited to a maximum total dose 100 Mrad and to a fluence of 3e15 n.eq./cm$^2$. For TFPX and TEPX, the opto-boards will be located at the periphery of the dee structures as shown in Fig. 9 (right), while for the barrel, there are three potential locations at higher radii available and under investigation. The first prototype opto-board is expected to become available in 2019 and will allow further studies on the mechanical constraints regarding their mounting location.

### 3.6 Data, Trigger and Control board

A compact 10 Gbps optical link sends out the data from the on-detector opto-boards to the back-end electronics, as shown in Fig. 10 (left). Readout links (shown in green and blue arrows) are

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carrying data from L1 accept and monitoring information to the DAQ and control system, control links (shown in pink and red arrows) are used to send clock, trigger, commands, configuration data to the pixel modules. A dedicated IT Data Acquisition (DAQ) Interface board, of ATCA format, called DTC (Data, Trigger and Control) will be used to readout the data and send them to the central DAQ or the luminosity processor, depending on the type of trigger.

Each DTC has two "half-DTC" FPGAs, each of which can receive up to 36 fibres. Twenty-eight DTCs will be needed to readout the entire IT. A mini-version of the DTC is being developed in uTCA format, called uDTC, shown in Fig. 10 (right). It is based on the FC7 [9] readout board and a new mezzanine card that has been developed to readout multiple prototype RD53A chips with full speed readout of the four Aurora lanes of the chip. The first ATCA DTC board is under development and will be delivered in 2019. In the meantime, the uDTC will be used for system tests and will provide useful feedback for the design and the required resources of the DTC.

## 4. Conclusions

The Phase-2 CMS Inner Tracker detector development is facing many challenges. In this paper, the key design choices and milestones of the R&D developments in 2018 have been presented. A new layout with extended forward coverage has been proposed, with TEPX design being currently optimised and proposed to be used also for luminosity and background measurement. Promising results from the sensor R&D campaigns have been achieved within the past year, while the first prototype RD53A chip has demonstrated full functionality and met specifications. The RD53A chips have been used across all fronts of development, including the HDI design for RD53A quad-modules. Many hardware developments have been done, including a lightweight carrier board for test-beams, low-mass electrical links, system tests of serial powering and a new mezzanine board for the uDTC. In addition, the first prototypes of mechanical parts made of carbon-fibre have been fabricated.

Important achievements are expected during 2019. Tests of irradiated prototype sensors in beams will provide a quantitative assessment of their longevity at HL-LHC, and guide the final sensor design, including choice of pixel aspect ration and spark protection method. The final CMS readout chip will be submitted by the end of this year and the first RD53A quad-modules with sensors will become available for system tests. These tests will allow for the optimisation of the serial powering scheme and to address potential system issues. In addition, the first prototype opto-boards and DTC boards are expected to be available in the summer 2019. By the end of the year, a complete readout chain will be completed with RD53A quad-modules, prototype e-links, opto-boards and a uDTC readout system that will pave the way towards the final electronics system.

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