PROCEEDINGS OF SCIENCE

The LHCb VELO Upgrade

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The LHCb experiment is a forward spectrometer experiment located at CERN, dedicated primarily to study CP violation and rare decays of beauty and charmed hadrons. The LHCb experiment will be upgraded during the current shutdown (2019-2020) to a trigger-less system reading out data at 40 MHz event rate. To cope with the higher data rates and increased occupancy, the LHCb sub-detectors including the VErtex LOcator (VELO) need to be upgraded. The VELO is a Si microstrip detector that surrounds the interaction region and performs highly precise track and vertex reconstruction. The microstrip sensors in VELO will be replaced by hybrid pixel sensors having $55 \times 55\ \mu\text{m}^2$ pixels, that are bump-bonded to VeloPix ASICs. Module will be cooled by circulating evaporative CO_2 coolant through microchannels etched in the Si substrate that provides mechanical support to the module components. The detector modules will be separated from the beam vacuum by 250 μm thick RF foil. Electrically working module prototypes have been built and rigorously tested at the assembly sites and at CERN SPS testbeam. This paper discusses the module components and design, electronic architecture, recent results and the current status of the VELO upgrade.

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1. Introduction

LHCb [1] (Figure 1) is an experiment that was designed to discover new physics through precise measurements of CP violation and rare decays of B and D mesons. It consists of various sub-detectors for charged and neutral particle detection. LHCb has been operational since 2009 and has been taking data from p-p collisions at an instantaneous luminosity of 4 $\times 10^{32}$cm^{-2}sec^{-1}. Till the end of LHC Run-2, it has accumulated about 9.6 fb^{-1} data. Its physics program has been highly successful. Still, many crucial analysis are statistically limited where the theoretical uncertainties are much smaller than the current experimental precision. The experiment is being upgraded to boost the luminosity to 2 $\times 10^{33}$cm^{-2}sec^{-1} and to collect upto 50 fb^{-1} data by the end of Run-4(in 2029). This will increase the analysis precision and may also help to constrain various new physics models. The hardware trigger will be replaced by a fully efficient software trigger having 40 MHz readout rate. Operating the detector at 40 MHz readout requires major upgrade in the LHCb sub-detectors and the detector readout system.

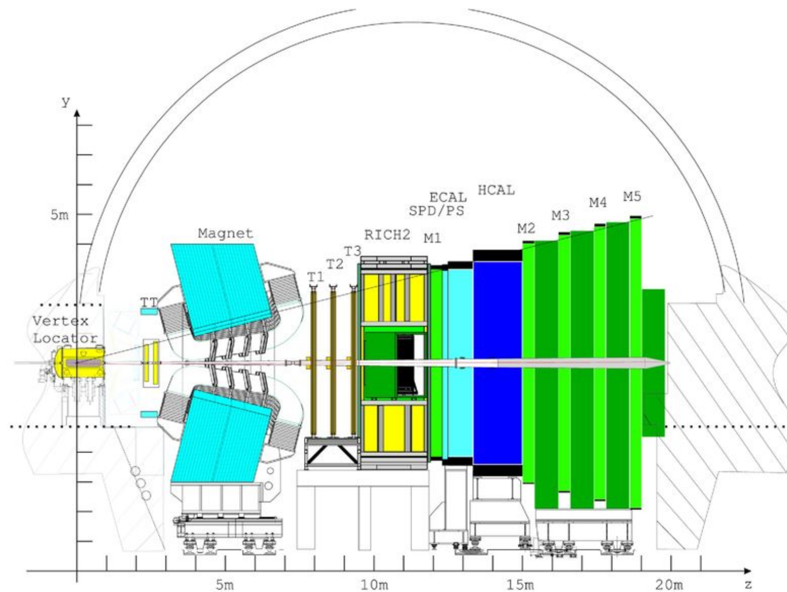

Figure 1: *The LHCb detector.* ©*CERN.*

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2. The Current VELO

The VErtex LOcator (VELO) [2] (shown in Figure 2) is the innermost sub-detector of LHCb. It consists of 42 modules consisting of semicircular Si microstrip detectors (300 microns thick, n^+ on n) arranged perpendicular to the beam along a length of ~1m. The modules are placed in two retractable halves inside the LHC beam pipe separated from the beam vacuum by 300 μm thick RF foil. Its corrugated shape allows overlap between the 2 detector halves in stable beam position and also reduces the material traversed by the particles. The active Si lies just 8.2 mm away from the LHC beam. Each module consists of a single sided radial (R) and an azimuthal angle (ϕ) measuring sensor mounted back-to-back on either side of a thermally conductive substrate. Each module thus

records a single R-ϕ space point. The sensors have a variable pitch. Evaporative CO_2 coolant circulates through stainless steel pipes that are embedded within the cooling blocks clamped to the base of the substrate. Data from the sensors are read out via the Beetle ASICs [3], which are then transmitted via analogue links to the repeater boards (through the vacuum feedthorough). Data is then transmitted via 60m long differential link to the off-detector FPGA based readout board (TELL1) [4]. Pedestral subtraction, common mode corrections and cluster finding are all performed on TELL1. The channel noise varies with strip pitch. Signal/noise ratio of ∼18-22 is maintained across all modules. The track finding efficiency of the current VELO is above 98 % and the impact parameter resolution is less than 35 microns for particles having transverse momentum $>$ 1 GeV/c. More information about current VELO performance is available in [5].

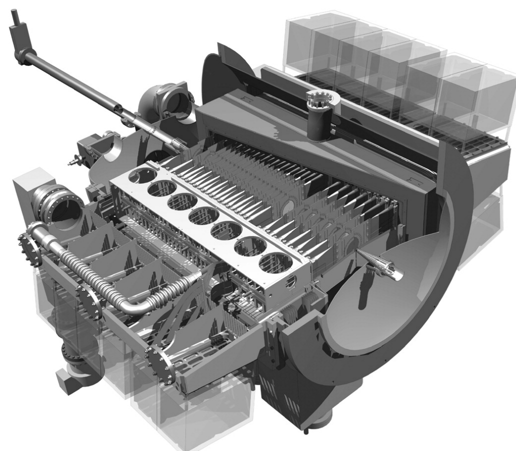

Figure 2: *3D CAD model of the current VELO [7]. The beam passes through the centre.*

3. The VELO Upgrade

The VELO requires a significant change to sustain the rigorous experimental challenges due to the increased luminosity and readout rate. The microstrip sensors will be replaced 200 μm thick pixel sensors bump-bonded to 3 VeloPix ASICs [6], each having dimensions $\sim 16\times 14$ mm^2. The sensors were chosen on the basis of testbeam studies reported in [7, 8]. The upgrade module (shown in Figure 3) consists of a 500 μm thick Si microchannel substrate supported by carbon-fibre legs and midplate. CO_2 coolant will be circulated through the microchannels to cool down the modules. Cooling pipes will route the CO_2 coolant to and from the cooling connector that is soldered to the substrate. The microchannel substrate also provides mechanical support to the different components. Two bump-bonded sensors are attached on either side of the substrate in an L shaped geometry with a slight overlap between them. Kapton hybrids consisting of discrete electronics and the GBTx chip [9] for control, power, bias and readout are also glued to the module. The z position of the modules were optimised based on simulation studies [10] that uses the criteria that 99% tracks should pass through at least 4 active sensors. The detector will consist of 52 modules positioned much closer to the beam (at R=5.1mm) and enclosed within a thinner (250 μm) RF foil. The design and thickness of RF foil was optimised for the upgrade. The module needs to be strong enough to withstand the mechanical stress, high pressure, sudden thermal shocks and

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repeated thermal cycling expected during its transport and operation. Various pressure tests were done before finalizing the micro-channel technology. The distortions due to thermal cycling should be within acceptable limits. Simulation studies and tests confirm this. Table 1 lists the major changes for the upgrade. Simulations for the VELO upgrade using the nominal upgrade luminosity ($2 \times 10^{33}\ cm^{-2} sec^{-1}$) estimate that the tracking efficiency will be much higher in the upgrade compared to the current VELO. The IP resolution will also be significantly improved, particularly for tracks with low transverse momentum. The findings are summarised in [11].

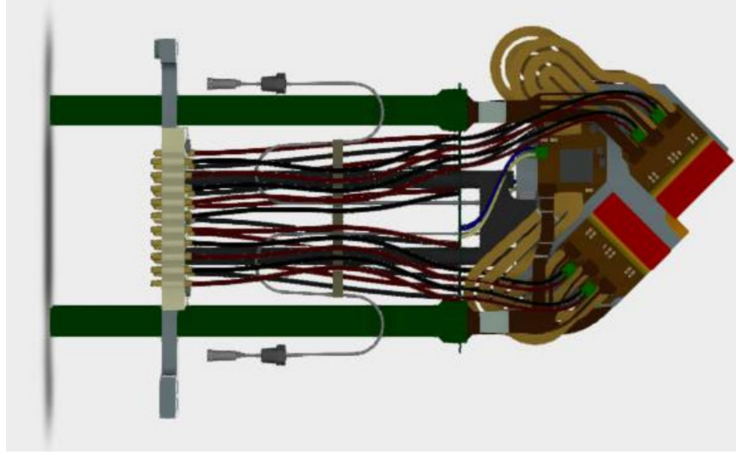

Figure 3: *VELO Upgrade Module (HV cables not shown).*

Feature	Current VELO	VELO Upgrade
Sensor	R and ϕ strips 300 μm thick 0.22 m^2 ~0.2 M Semicircular	pixels 200 μm thick 0.12 m^2 41 M L shaped geometry
Distance from beam	8.2 mm	5.1 mm
Maximum Fluence	5.2×10^{14} 1 MeV neq cm^2	8×10^{15} 1 MeV neq cm^2
HV Tolerance	500 V	1000 V
No. of modules	42	52
ASIC readout rate	1 MHz	40 MHz
Total data rate	~150 Gb/sec	2.8 Tb/sec
Power consumption	~16.5 W/module	~28 W/module
Operating temperature	< -10°C	< -20°C
RF foil thickness	300 μm	250 μm

Table 1: *The Changes in the upgrade.*

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3.1 Silicon Sensors

For the upgrade, 200 μm thick Hamamatsu n-on-p Si pixel sensors were chosen. The sensors having an active area of 42.57 $\times$ 14.08 mm^2 will be bump-bonded to 3 readout ASICs. The size of the sensor pixels matches with the ASIC pixels (55 $\times$ 55 μm^2) except in the gaps between the ASICs (where the pixels are elongated). A series of beamtests [7, 8] were done at CERN SPS testbeam using Timepix3 telescope [12] to select the sensor on the basis of sensor technology, dopant type, thickness, edge distances, guard ring designs, implant size and the readout electronics. Prototype pixel sensors from two vendors (Hamamatsu and Micron) were tested upto full fluence irradiation (8 $\times$ 10^{15} MeV neq/cm^2). Testbeam results shows that the irradiated sensors satisfy the desired charge collection criteria, can function with a bias voltage of upto 1000 V and still retain a hit efficiency of 99%. Results and plots are presented in [7, 8].

3.2 Cooling

The increased luminosity and the close proximity of the sensors to the beam will lead to an increase in the hit occupancy in the sensor and a greater power consumption in the front-end ASICs necessitating a highly efficient cooling. The part of the Si sensors close to the beam is most vulnerable to radiation damage. The coolant and the cooling structure should consist of minimal material. Further, it must be able to maintain all regions of Si sensors below -20 °C and dissipate anticipated 28 W power, throughout the lifetime of the experiment to minimize the chances of thermal runaway. The microchannel technology and Si substrate is chosen after dedicated studies reported in [13]. Modules will be cooled by circulating evaporative CO_2 through miniature channels etched within the Si substrate [13]. The CO_2 connector with the welded pipes are soldered to the microchannel substrate. The inlet fans out to a series of parallel microchannels which routes the coolant directly under the site of the heat sources (the GBTx chip and the VeloPix ASICs) to minimise the temperature gradient across the module. The microchannels form a restriction region of higher pressure near the inlet, followed by a transition region where the channels widen from 60 μm $\times$ 60 μm to 120 μm $\times$ 120 μm stimulating boiling of the CO_2. These restrictions are essential to equalise the flow and to prevent coupling between the channels. The expected pressure drop over the substrate is $\sim$5 bar. The microchannel layout is optimised in terms of structural integrity, cooling and pressure performance requirements. Microchannel substrate assemblies are quality assured by simulteneous thermal cycles and pressure tests upto 186 bar.

3.3 RF Foil

The RF foil shields the front-end electronics from RF frequency pick-up due to beam currents and the beam from module outgassing. The foil will be milled from a $AlMg_3$ block with its thickness aimed to be 250 μm. It is aimed to place the foil as close to the beam as possible so as to enable closer placement of the sensors. The foil is expected to be able to withstand radiation doses of up to 1000 MRad. The shape and thickness of the RF foil is changed substantially to accomodate the upgraded sensors. The first RF box prototype has been milled with a mechanical positioning accuracy $<$ 100 microns and thickness uniformity of 100 microns.

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3.4 VELO Electronics Architecture

The higher luminosity and closer proximity of the sensors to the beam will lead to higher hit occupancy in the sensors. The innermost ASIC will see an average 8.5 tracks per bunch crossing at the nominal upgrade luminosity. The VeloPix readout chips [6] (based on TimePix3 [14]) used for the upgrade has a binary, data driven readout. It consists of a 256 $\times$ 256 pixels having pixel dimensions 55 $\times$ 55 μm^2 to match the sensor. The binary hit information will be time stamped, addressed and will be read-out as super-pixel (SP) packets (group of 2 $\times$ 4 pixels) to reduce the output bandwidth by $\sim$ 30 % over standard pixel readout. Each time a pixel within the SP packet records a signal above the threshold, a hit packet will be generated and propagated along the column shift register to the end of column logic. The hit packet will contain the address, the hit pattern and the bunch ID information of the super-pixel. The readout will vary as a function of SP hit position. Hits closer to the beam will take longer to reach the end-of-column readout logic. Further, the hits will be disordered in time. Figure 4 shows the block diagram of VeloPix.

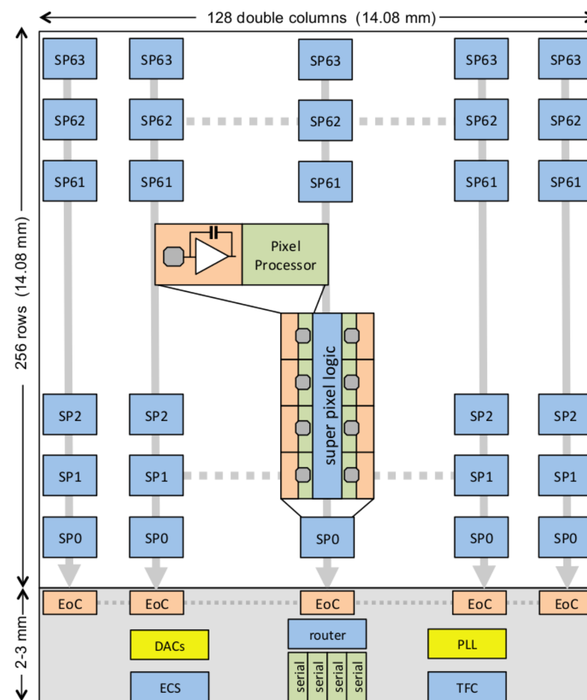

Figure 4: *VeloPix ASIC Architecture. [6]*

The ASICs will be wirebonded to the front-end hybrids. The hit packets from all columns will be collected and serialised into four high speed serial links running at 5.12 Gbit/sec. The data will pass through the vacuum feedthrough to the OPB board which will convert the electrical signals to optical signals and will send them to the PCIe40 board [15]. The PCIe40 board is a generic readout board for the LHCb upgrade. Its firmware is described in [17]. The GBTx hybrid will provide clock, control and configuration information to the VeloPix ASICs and will also read back monitoring information from the ASICs. The electrical links and power cables are designed to be flexible enough to absorb the stress due to motion of the module halves during each LHC fill. The

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complete electronic chain is shown in Figure 5.

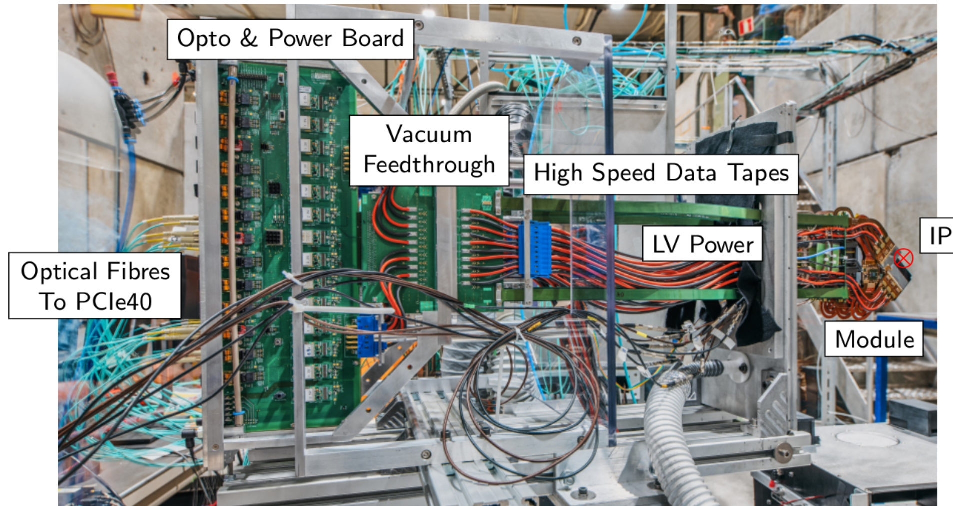

Figure 5: *Prototype Readout Chain at CERN SPS Testbeam. [18].*

3.5 Current Status

Production grade modules are being assembled and tested at both the assembly sites (Nikhef and University of Manchester). Highly precise jigs (∼ few tens of microns) are machined for module assembly. Tiles, hybrids and all electronic components are checked for flatness, residue, damage, bad solder quality, etc. Planarity of the substrate and the position of tiles and hybrids are measured with the smartscope. Small non-uniformities in the substrate (∼ 20-30 microns) will be accomodated within the glue layers. The aligment precisions of tiles and hybrids are measured to be around or within the desired ∼20 microns and ∼100 microns respectively. Wirebonds were optimized by pull testing on dummy and prototype modules. The bond strength measured on the sacrificial bonds averages well above the desired 5g pull force.

For electrical and thermal tests, the fully assembled module (with the full readout chain and cabling) is placed in a tank and the tank evacuated to $< 10^{-3}$ mbar pressure. The module is then cooled down to -30°C by circulating CO_2 through the microchannels. Communication between the readout ASICs and the MiniDAQ directly and via GWT is checked by sending test pulses and random binary sequence (PRBS). ECS lines are tested using equalization and noise scans. TFC is tested using TFC signals. Quality of the sensors and ASICs are checked by measuring the IV curves, noise maps and threshold scans. Thermal performance of the module is tested using bandgap measurements. The module is thermal cycled (from -30°C to +20°C and back) several (10) times and the wire-bonds pull-checked thereafter to ensure that the connections are good enough for long term module operation. Distortions in the module induced due to temperature variations is monitored with the displacement sensors connected to the test frame. The hybrid temperature and voltages on the sensors and ASICs were monitored during the tests. The modules must satisfy the desired electrical criteria for qualification. Three electrically working prototype modules were arranged linearly and placed perpendicular to 120 GeV pion beam at CERN SPS testbeam [18] and data is recorded. This allowed a complete test of the DAQ and the software chain with real data.

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Figure 6 shows the beam hitmap in an ASIC lying on the first module layer. The beam spot can be clearly seen in the ASIC. Few (5) production grade modules have been assembled, tested and electrically qualified at the assembly sites as of August 2019. Full set of (52) modules are expected to be assembled by April 2020.

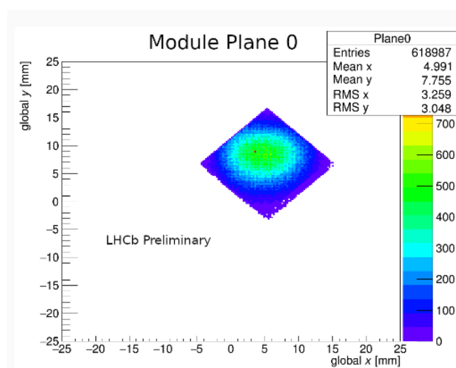

Figure 6: *Beam hitmap on an ASIC lying on the first module layer at the testbeam.*

4. Summary and Conclusions

The VELO will undergo significant improvement to operate at the high luminosity environment during Run-3. The upgraded VELO will be commissioned during the current shutdown LS2. The assembly and testing of prototype modules is currently ongoing and is progressing well. Electrically working prototype modules were successfully tested at CERN testbeam. Few production grade modules were assembled and qualified for commisioning. Sufficient production-grade modules are expected to be assembled by April 2020 to start commisioning.

5. Acknowledgements

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