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Status of silicon detector R&D at CLIC

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The Compact Linear Collider CLIC, a multi-TeV linear electron-positron collider, aims at precision measurements of the Standard Model, as well as direct and indirect searches of physics beyond the Standard Model. These aims translate into challenging requirements imposed on the detector. To reach these requirements, a silicon tracking system is envisaged, being composed of a low-mass vertex detector and a large scale tracker. While the requirements on the tracker are mainly driven by the need for a precise momentum resolution, the requirements on the vertex detector are mainly motivated by the demand on reconstructing secondary vertices from heavy-flavour quarks. A single point spatial resolution of a few micrometres is required for the tracking system together with a material budget of 0.2 % of a radiation length per detection layer in the innermost layers. To mitigate hit rates from beam-induced background particles, a timing resolution in the order of a few nanoseconds is needed and the cell sizes are restricted down to $25 \times 25\,\mu\text{m}^2$ in the vertex detector and $25\,\mu\text{m} - 10\,\text{mm}$ in the tracker. To evaluate which technology can meet these requirements, a broad silicon detector R&D is performed for a selected choice of technologies.

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1. Introduction

To achieve high precision measurements at the Compact Linear Collider CLIC, a multi-TeV linear electron-positron collider, challenging requirements are imposed on the detector [1, 2]. An all silicon tracking system is under development, composed of a low-mass silicon vertex detector and a large scale ($\sim 140\,\mathrm{m}^2$) silicon tracker. Driven by the requirement of a precise momentum resolution, a material budget of $1-2\,\%\,\mathrm{X}_0$ per detection layer together with a spatial resolution of $7\,\mu$m is needed for the tracker. For the CLIC vertex detector a material budget of $0.2\,\%\,\mathrm{X}_0$ and a spatial resolution of $3\,\mu$m are required to reach the required resolution for secondary vertices. Moreover, a timing resolution of ~ 5 ns is needed in the full tracking system to mitigate effects from out-of-time background hits from beam-induced background particles.

The low repetition rate of 50 Hz of the colliding bunch trains at CLIC allows the front-end electronics to be powered down during the time between the bunch trains. By this, the heat dissipation can be reduced to a level that allows for forced air-flow cooling of the vertex detector. Using air instead of liquid cooling significantly reduces the material budget in the vertex detector.

A selective choice of technologies is developed and evaluated to find technologies that can simultaneously meet all challenging requirements for the CLIC vertex detector and tracker. Silicon pixel detector technologies with a readout chip separated from the active sensing layer (hybrid technologies) allow to optimise the readout functionality while not affecting the sensing part of the detector. This is especially relevant for the CLIC vertex detector where functionality meeting the demanding requirements must be implemented in a small pixel size of around $25\,\mu$m. To overcome the production effort and costs of interconnects between the sensor and the readout ASIC (particularly for the large area CLIC tracker) and to reduce the material budget, monolithic technologies with the circuitry integrated in the sensor are attractive candidates.

This paper presents results of the study of various silicon pixel detector technologies, focusing on the research on monolithic Complementary Metal-Oxide-Semiconductor (CMOS) sensors with a small collection electrode.

2. Hybrid technologies

In the following, hybrid prototypes with chips specifically designed for the CLIC vertex detector, various sensors and different interconnects are discussed.

2.1 CLICpix / CLICpix2

The CLICpix 65 nm CMOS chip [3], has been produced with a pixel size of $25\mathrm{x}25\,\mu\mathrm{m}^2$, targeting specifically the stringent requirements for the CLIC vertex detector. The CLICpix readout ASIC is a chip of the Timepix/Medipix chip family [4] with a simultaneous 4-bit Time over Threshold (ToT) and 4-bit Time of Arrival (ToA) readout, using a 100 MHz clock. A second version of the chip has been produced with 5 bit ToT, 8 bit ToA precision and improved noise isolation (CLICpix2).

2.2 CLICpix assemblies and test-beam results

The CLICpix readout ASIC has been bump-bonded by SLAC to planar sensors with a thickness of $50\,\mu$m, $150\,\mu$m and $200\,\mu$m [5]. Test-beam results have shown that for the $200\,\mu$m thick

sensors a spatial resolution close to the 3 μm required for the CLIC vertex detector can be achieved [6]. However, for the 50 μm thin sensors that fulfil the low-mass requirement for the CLIC vertex detector, the spatial resolution is degraded to $\sim$ 8 μm due to the reduced charge sharing in thin sensors [7].

CLICpix2 ASICS have been bump-bonded by IZM to active-edge planar sensors with a thickness of 100 μm, 130 μm and 150 μm [8]. The cross section of a bump-bonded assembly depicted in Figure 1 shows a good physical separation of the fine pitch bump-bonds. Test-beam data have been recorded and are currently being analysed.

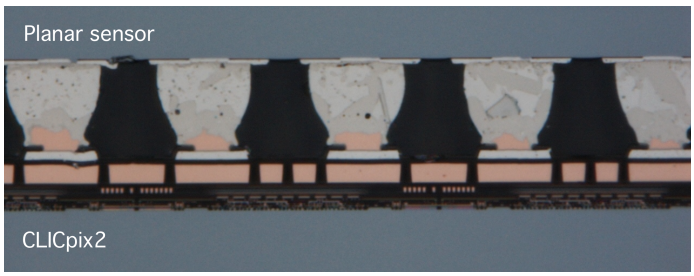

Figure 1: Cross section picture of CLICpix2 bump-bonded to a planar sensor [8].

An alternative concept avoids the challenge of fine pitch single-chip bump bonding by using the capacitive coupling of the CLICpix ASIC to the sensor via a layer of glue. To achieve a signal in the sensor that is high enough to be transferred to the readout ASIC via the capacitive coupling, High-Voltage (HV) CMOS sensors that integrate first amplification stages inside a large collection electrode have been used. The bias voltage is applied to implants on the front side of the sensor next to the collection electrode, limiting the achievable depletion depth compared to designs with a separate bias voltage contact on the back side of the sensor. Figure 2 shows a cross section of the electric field in such a CMOS sensor, calculated using finite element Technology Computer Aided Design (TCAD) simulations [9]. As visualised by the white line in Figure 2 that marks the edge

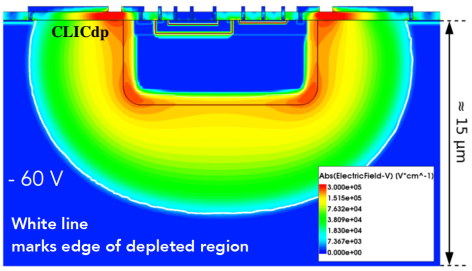

Figure 2: Electric field of a CMOS sensor with a large collection electrode simulated using TCAD [9].

of the depleted region, only part of the sensor is depleted for the given bias voltage of -60 V and substrate resistivity of 10 Ωcm. Therefore, contributions from drift are expected from the charge carriers propagating in the depleted regions, while a contribution from diffusion is expected from charge carriers randomly propagating through the non-depleted regions of the sensor.

To understand and disentangle the contributions from drift and diffusion to the overall response, test-beam studies have been performed for particle tracks passing through the sensor with

varying incident angle with respect to the sensor surface. Figure 3 presents the mean cluster size for different incident angles. Using basic geometrical considerations, the active depth of the sen-

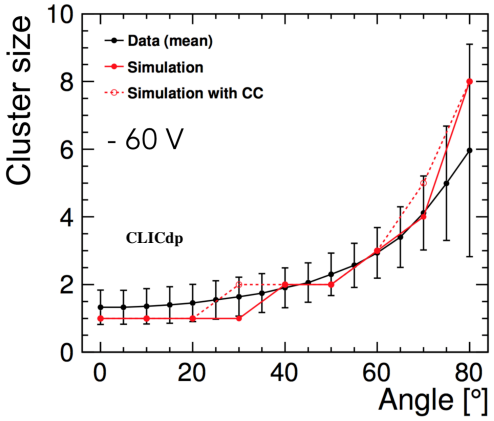

Figure 3: Mean cluster size along inclination versus inclination angle [9]. The uncertainties are the RMS of the cluster size distributions.

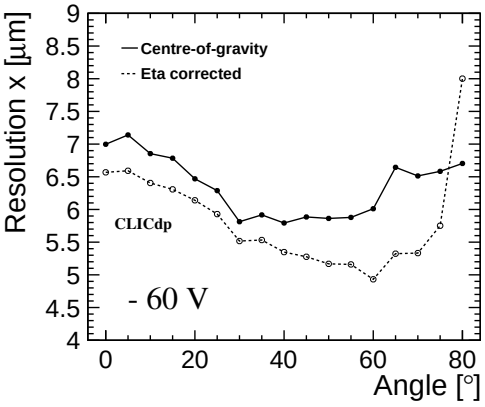

Figure 4: Resolution along inclined dimension versus inclination angle [9] for different reconstruction methods.

sor has been calculated to be $\sim 30\,\mu$m, significantly larger than the simulated depletion depth of $13\,\mu$m [9]. Thus, one can conclude that a significant contribution of the measured charge originates from the non-depleted regions of the sensor.

Figure 3 shows also that only a small fraction of the charge is shared at particle incident angle of 0°. This is attributed to the high and homogenous electric field in the sensor and reflected in the measured spatial resolution that is shown as a function of the particle incident angle (see Figure 4). A spatial resolution of $\sim 7\,\mu$m has been achieved for perpendicular particle incidence.

2.3 Enhanced lateral drift sensors

To enhance the charge sharing and thereby improve the spatial resolution for a given pixel size and thickness, sensors with additional deep implants have been studied. These Enhanced Lateral Drift (ELAD) sensors use deep implants to shape the field lines in the sensor such that more charge is shared between the pixels. TCAD and Geant4 based Monte Carlo simulations indicate a significant improvement in resolution and first test-structures of ELAD sensors with various deep implant doping values are currently in production [10].

3. Monolithic technologies

Several monolithic technologies are investigated in the context of the CLIC silicon pixel R&D. While results for monolithic HV CMOS technologies with a large collection electrode are summarised elsewhere [11], studies on integrated technologies with an insulation layer between the sensor and the readout part as well as integrated technologies with a small collection electrode are discussed in the following sections.

3.1 SOI CMOS

Silicon On Insulator (SOI) technologies integrate the readout circuitry as an additional layer on top of the sensor surface which is separated from the active sensor volume by a buried oxide layer. Avoiding an additional interconnection layer between sensor and circuitry makes this technology attractive in view of material budget and interesting for the vertex detector to avoid small pitch bump-bonding.

SOI prototypes have been produced in a 200 nm SOI CMOS LAPIS process and tested in various test-beam campaigns [12]. As presented in Figure 5 and Figure 6, test-beam results of sensors with a pixel size of $30 \times 30\,\mu\text{m}^2$ and a thickness of $500\,\mu\text{m}$ show good performance with an efficiency of $\sim 98\,\%$ and a spatial resolution down to $\sim 3\,\mu\text{m}$. To meet the material budget

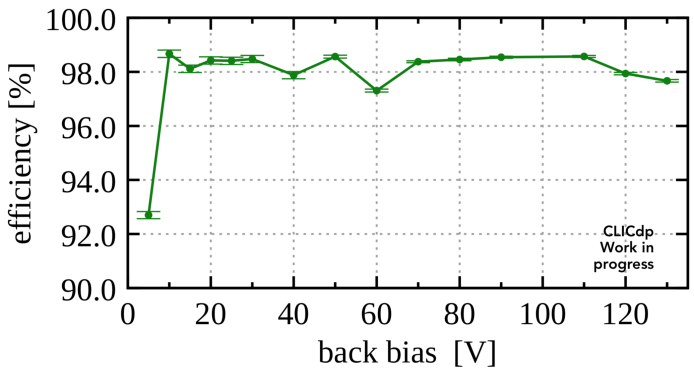

Figure 5: Efficiency versus back side bias voltage.

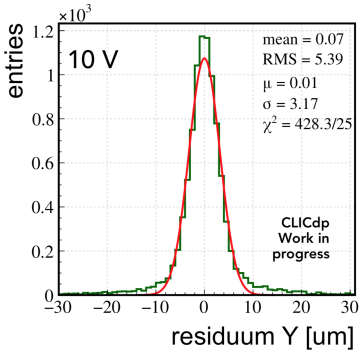

Figure 6: Residual distribution.

requirement for the vertex detector, a fully integrated SOI chip, the CLIPS [13], with a pixel size of $20 \times 20\mu\text{m}^2$ has been produced. It can be thinned down to $100\,\mu\text{m}$.

3.2 CMOS sensors with a small collection electrode

As presented in Figure 7 (left), CMOS sensors with a small collection electrode incorporate the circuitry in a shielding implant (well) in the sensor that is inversely doped and separated from the collection electrode. By this, the sensor capacitance can be minimised to a few femto-Farads [14],

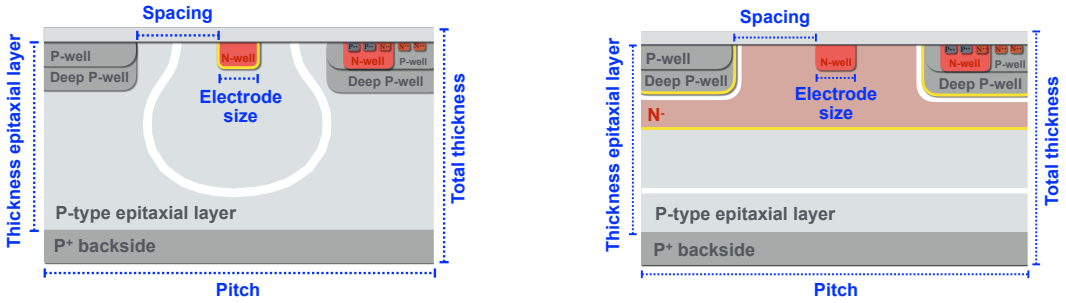

Figure 7: Schematic cross section (not to scale) of the standard (left) and modified (right) CMOS process with a small collection electrode. The white lines mark the edges of the depleted regions, the yellow lines the junction.

allowing for a low detection threshold down to $\sim 10 e^-$ and a good signal to noise ratio [15]. All implants are placed on a high resistivity epitaxial layer to maximise the size of the depleted region. To achieve full lateral depletion, the sensor has been modified by inserting an additional low dose deep n-implant [16], as illustrated in Figure 7 (right).

The Investigator analogue test-chip produced in a 180 nm CMOS imaging process has been investigated in various test-beam campaigns [15]. Different sensor layouts have been studied for the standard and modified process with a pixel size of 28 μm. The results of two-dimensional TCAD simulations of the electric field are presented in Figure 8.

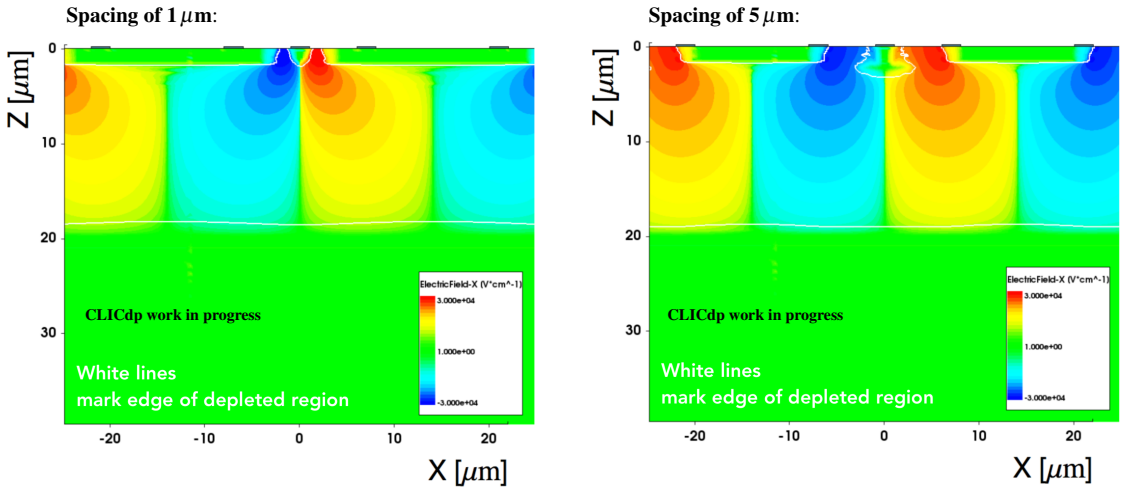

Figure 8: Electric field in the transverse sensor direction X from 2D TCAD simulations for a spacing of 1 μm (left) and a spacing of 5 μm (right) [15].

The higher electric field for larger spacings results in less charge sharing and thus a degraded spatial resolution and larger efficient operation window, as well as a faster charge collection compared to the smaller spacing (see Figure 9). Thus, an intermediate spacing of 3 μm has been found

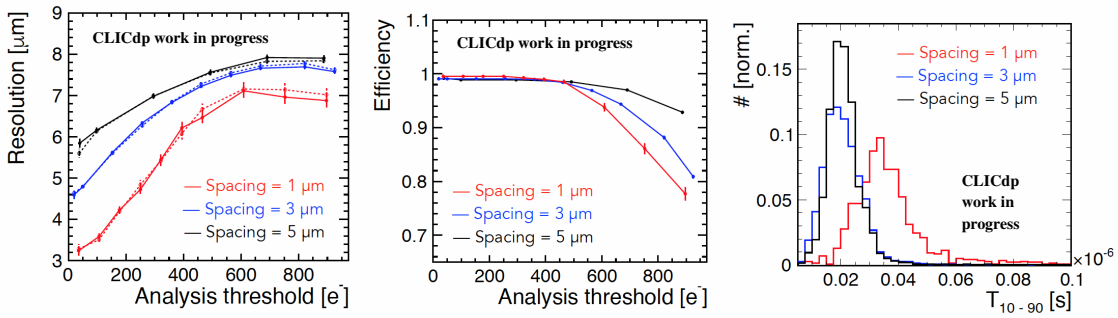

Figure 9: Resolution (left), efficiency (middle) and charge collection time (right) obtained in test-beam measurements of sub-matrices of the Investigator test-chip with different distances between the collection electrode and P-well (spacing) [15].

to be a good choice to maximise the global performance.

Overall, the test-beam results show that the requirements for the CLIC tracker can be reached in terms of analogue performance for a pixel size of $28 \times 28\,\mu m^2$ [15]. This triggered the design

of a fully integrated chip in this technology for the CLIC tracker, the CLICTD [17]. The CLICTD has been designed using elongated pixels with the dimensions of $30\,\mu\text{m} \times 300\,\mu\text{m}$. Each elongated pixel contains 8 sub-pixels with a size of $30\,\mu\text{m} \times 37.5\,\mu\text{m}$, to ensure prompt charge collection in the sensor. The discriminated output of all sub-pixel is combined in a common digital front end by means of an OR-gate. The charge per sub-pixel is integrated by a charge sensitive amplifier and a global threshold is applied that can be tuned individually for each sub-pixel. In nominal operation mode the ToT of the sub-pixel with the highest signal and the ToA of the earliest sub-pixel are read out using a 100 MHz sampling clock, together with the hit-pattern of the sub-pixels.

Electrostatic three-dimensional TCAD simulations are performed to obtain a description of the highly non-uniform electric field in the sensor. The solution of the electric field from TCAD can then either be used to further perform a simulation of a particle incident with a detailed time-resolved transient-current simulation using TCAD or as input for high statistics Monte Carlo simulations. To investigate if the charge is collected sufficiently rapidly in the CLICTD pixel, transient three-dimensional TCAD simulations have been performed. The worst case scenario in view of charge collection time has been benchmarked, by simulating a Minimum Ionising Particle (MIP) traversing the pixel corner at the farthest distance from the collection electrodes, where the low electric field regions are located. The transient current result for the standard and modified processes are depicted in Figure 10, showing the severely degraded charge collection time of the standard with respect to the modified process.

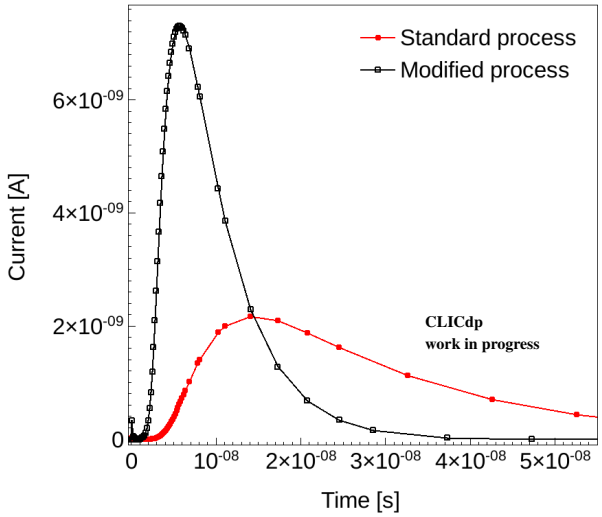

Figure 10: Current pulse for a MIP traversing the pixel corner for the standard and modified process.

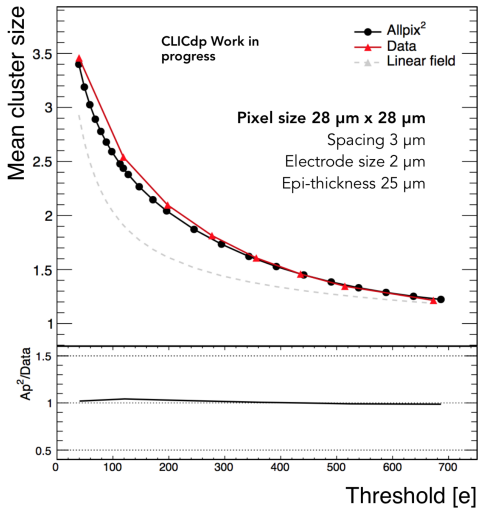

Figure 11: Mean cluster size versus threshold for data and AllpixSquared simulations.

Moreover, the electric field distributions have been integrated in Monte Carlo simulations to produce high statistic event samples. AllpixSquared [18], a modular Monte Carlo silicon pixel detector simulation framework based on Geant4, has been developed within the CLICdp R&D effort. Figure 11 shows the comparison of the AllpixSquared simulation with a linear electric field assumption and using the electric field simulated for the standard process to test-beam data [19]. The measured mean cluster size is described very well by the simulation, which makes use of a simplified model where charges that physically arrive at the collection electrode are counted. As

illustrated by the large discrepancy between the linear electric field assumption (grey dashed line) and the measured test-beam data, a detailed modelling of the electric field in TCAD is essential to describe the measured performance.

4. Conclusions

To reach the challenging requirements for the CLIC tracking system, a broad R&D programme is performed, studying in detail various selected technologies. A 25 μm pitch readout ASIC, the CLICpix, has been designed specifically to address the requirements for the CLIC vertex detector. CLICpix and CLICpix2 chips have been bump-bonded to planar sensors, showing the difficulty of meeting the low material budget together with the precise spatial resolution required for the vertex detector. CLICpix chips capacitively coupled to active HV-CMOS sensors via a layer of glue show the challenge of reaching the spatial resolution requirement for the CLIC vertex detector. Enhanced Lateral Drift sensors are currently under development, using deep implants to shape the electric field such that more charge sharing can be achieved for a given pixel geometry.

Test-beam results of SOI prototype chips show promising performance results and a fully monolithic chip has been produced in this technology, targeting the requirements for the CLIC vertex detector. Test-beam and simulation studies have been performed to investigate the analogue performance of CMOS sensors with a small collection electrode. The results show that this technology is an attractive option for the CLIC tracker and motivate the design of a fully integrated chip in this technology.

Various simulation studies are performed for complex structures such as integrated CMOS sensors, ranging from transient three-dimensional TCAD simulations to Monte Carlo simulations that include the description of the TCAD electric fields.

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