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Review on depleted CMOS

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Monolithic active pixel sensors (MAPS) integrate both sensor matrix and readout circuitry in one piece of silicon. Pixel sensors in commercial CMOS technologies receive increasing interest for vertex and tracking detectors. They have advantages in detector assembly, production cost, and other benefits like lower material and higher granularity. Used for the first time in the STAR experiment, adopted for the ALICE experiment, they are being considered for future detectors, like the ATLAS HL-LHC upgrade, FCC and CLIC. The most aggressive applications require full depletion in the sensing volume where charge collection by drift improves timing and radiation tolerance to high-intensity hadron fluences. This paper addresses the improvements and challenges of depleted CMOS with insights on sensor and circuit design.

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1. Introduction

Silicon pixel sensors are used in tracking and vertexing detectors to provide a good spatial resolution of the incident charged particles close to the interaction point. Hybrid pixels consist of a pixellated sensor bonded to a CMOS readout chip, they are presently the technology used for the innermost layers of most high-energy physics experiments [1]. Monolithic active pixel sensors (MAPS) integrate the readout electronics and the sensing volume on the same silicon die. MAPS are produced in commercial CMOS technologies on a high resistivity substrate or lower resistivity substrate with a high resistivity epitaxial layer, and the charge generated there is collect. MAPS offer higher resolution and lower material in the vertex detector with a significant cost advantage. Standard CMOS processing allows to get access to large wafer diameter reducing the cost per area. The detector assembly is facilitated by the fact that there is no need for cost intensive fine pitch bump bonding.

Table 1 reports the requirements for detectors at different collider experiments.

	STAR RICH	ALICE-LHC	ILC	HL-LHC Outer layer	HL-LHC Inner layer	CLIC
Required time resolution [ns]	200 10^3	20 10^3	350	25	25	1
Particle Rate [kHz/mm^2]	4	10	250	10^3	10 10^3	< 0.3
NIEL Fluence [n_{eq}/cm^2]	$< 10^{12}$	$< 10^{13}$	10^{12}	10^{15}	10^{16}	$< 10^{12}$
Total Ionizing Dose [Mrad]	0.2	0.7	0.4	50	1000	1

Table 1: Detector requirements.

The time resolution depends on the convolution of the sensor charge collection time and the front-end response time. In the sensor undepleted volume the signal charge is collected by diffusion with a long collection time. In the sensor depleted volume the signal charge is collected by drift driven by the sensor reverse bias electric field, with a reduced charge collection time. The front-end response time is proportional to the sensor input capacitance and inversely proportional to the power dissipation on the amplification stage. Lower capacitance is not only beneficial for timing but also for Signal to Noise (S/N) optimization for a given power consumption. Indeed, the analog power consumption is determined by the required S/N ratio for a given bandwidth, $P \propto (S/N \cdot Q/C_{eff})^m$, $2 \leq m \leq 4$, where P is the power consumption, Q is the collected charge, and C_{eff} is the effective sensing node capacitance [3]. Low power consumption allows for a detector with low mass, reducing the material budget both for power cables and cooling system.

The pixel hit rate sets requirements on timing and read-out speed. A pile-up happens when a new hit comes during the processing time of the first hit: the circuit is not be able to distinguish the two events causing a hit information loss. To reduce the analog pile up probability, the front-end pulse duration has to be significantly shorter than the inverse of the pixel hit rate. To reduce the digital pile up probability, the hit information has to be transferred to the periphery in a short time. In-pixel multi-event buffers can be used to further reduce the digital pile-up for a given transfer speed.

MAPS combine circuit and sensor, and the circuit radiation tolerance is similar as for other CMOS circuits. The CMOS circuit is more sensitive to the ionizing radiation (TID). Ionization in the dielectric layers of the CMOS chip generates charge and interface states that modifies the transistors electrical characteristics. The general trend is that with scaling technologies get more radiation tolerant due to the reduction of the oxide thicknesses [4]. However each technology requires a dedicated TID characterization, with a similar procedure followed for CMOS technologies used for the readout chips for hybrid pixels [5]. If needed, some of the TID effects can be mitigated by radiation hardening by design techniques [6].

While CMOS circuits are more sensitive to ionizing radiation, silicon sensors are generally more sensitive to displacement damage by non-ionizing radiation (Non-Ionizing Energy Loss or NIEL). A review of silicon properties affecting charge collection after irradiation is presented in [7]. The probability to loose charge signal because of capture by radiation-induced defects or traps increases with charge collection time. A fully depleted sensor with fast charge collection time would be more tolerant to non ionizing radiation.

In traditional MAPS the epitaxial layer is not fully depleted and the charge collection time is dominated by the diffusion component. This is sufficient to achieve time resolution in the order of 100 ns and a radiation tolerance in the order of 10^{13} n_{eq}/cm^2. MAPS are now state of the art for experiments with moderate particle rate with no stringent timing requirement and moderate radiation environment.

For the experiments with more stringent timing and stronger radiation tolerance requirements, where hybrid pixels have been traditionally used, fully depleted monolithic active pixels (DMAPS) have been developed. To make MAPS radiation hard beyond 10^{13} n_{eq}/cm^2 the charge has to be collected by drift. The depletion depth w_d can be increased increasing the sensor reverse bias V_b and/or the resistivity of the epi layer ρ_{epi}, in case of a planar junction $w_d \propto \sqrt{\rho_{epi} \cdot V_b}$.

Integrating the sensor in the CMOS readout electronics layer poses some challenges. A proper signal isolation between the electronics and the sensing part is crucial. The signal has to be collected by the designated electrode without charge losses. In the following a review of different technologies and solutions is presented.

2. Non depleted MAPS in HEP

Monolithic pixels are very attractive for detectors that require high precision tracking of low momenta particles emerging from the interactions. The reduced material thickness reduces the multiple Coulomb scattering. This associated with a small pixel size allows to improve the detector position resolution. This sections covers the first non depleted MAPS for High Energy Physics experiments with moderate requirements on non ionizing radiation tolerance ($< 10^{13}$ n_{eq}/cm^2) and timing (> 100 ns).

2.1 The ULTIMATE sensor for the STAR experiment

The first vertex detector based on MAPS is the PXL sub-detector of the STAR experiment at the Relativistic Heavy Ion Collider (RHIC) [8]. It is equipped with the ULTIMATE CMOS pixel sensor, fabricated in a CMOS 0.35 μm OPTO process (Figure 1). It is a 2 cm $\times$ 2 cm chip thinned

down to 50 μm to reduce the material budget [9]. It has an active area of 3.8 cm^2 with 928 $\times$ 960 pixels with a pitch of 20.7 μm.

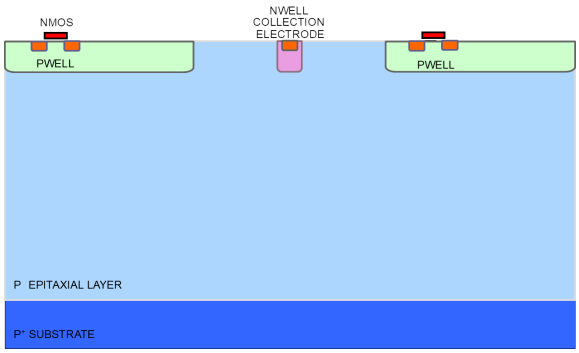

Figure 1: ULTIMATE pixel cross-section with n-well collection electrode on p-type epitaxial layer and p-wells housing NMOS transistors.

The collection electrode is a n-well in a 20 μm thick p-epitaxial silicon, grown on a highly doped p-substrate (Figure 1). The epitaxial layer resistivity is moderately high (> 400 $\Omega \cdot$ cm) compared with the standard value of 10 $\Omega \cdot$ cm. This creates a shallow depletion volume with an extension of few μm that reduces the junction capacitance to $\approx$ 10 fF. For the same bias conditions the signal to noise improves by a factor two. Inside the pixel only NMOS transistors are allowed, the n-well of PMOS transistors would act as a competing collection electrode.

The in-pixel circuit performs amplification and Correlated Double Sampling (CDS). The matrix is read-out in rolling shutter mode, as in the CMOS Image sensors. The columns are read out in parallel, the analog information of the selected row is buffered to a discriminator at the end of column. After readout the circuit is reset, the integration of the sensor signal occurs in the time between two read-out. Each row takes 200 ns, and the row by row read-out takes 185.6 μs for 928 rows. The limitation on minimum integration time set by the read-out speed makes this architecture not suitable to achieve significantly better time resolution.

2.2 The ALPIDE sensor for the ALICE experiment

A full in-pixel CMOS circuitry, with both NMOS and PMOS, is required for an architecture that removes the limitation on time resolution set by the read-out speed. The TowerJazz 180 nm CMOS imaging sensor process (Figure 2) introduced a deep p-well implant [10] to shield the n-well containing the PMOS transistors from the p-doped epitaxial layer. In this way the ionization charge signal is collected only by the designated collection electrode.

ALPIDE is the first MAPS in high-energy physics with sparse readout similar to hybrid sensors [11]. It was developed for the upgrade of the Inner Tracking System (ITS) of the ALICE experiment. The new ITS will be installed in 2020 and it will be the first detector at the LHC implementing a large (10 m^2) silicon tracker with MAPS [12] for a total of 12.5 10^9 pixel.

ALPIDE is a 3 cm $\times$ 1.5 cm pixels sensor chip thinned down to 50 μm to reduce the material budget. It has an active area of 3.8cm^2 with 1024 $\times$ 512 pixels with a pitch of 28 μm. It is implemented with the TowerJazz 180 nm CMOS imaging sensor process, featuring a 25 μm thick high resistivity epi-layer (>1 kΩ·cm) with possibility to apply reverse bias (-6 V) to the substrate. This

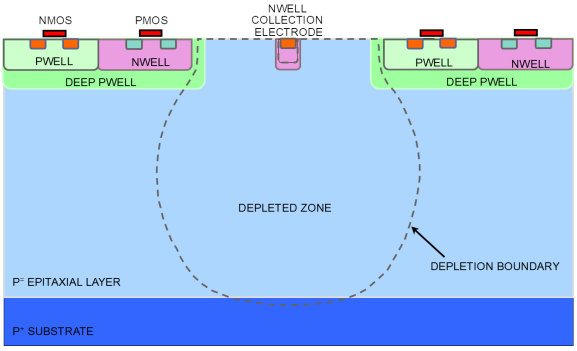

Figure 2: Pixel cross section in TowerJazz 0.18 μm CMOS imaging sensor process featuring deep-p-well.

increases the depletion volume around the n-well collection diodes reducing the sensor capacitance to 2.5 fF ([13]). However, the sensor depletion volume is limited to the region around the collection electrode and signal charge generated outside the depleted area is still collected primarily by diffusion. The in-pixel circuit [14] has a low power (40 nW) analog circuit that amplifies the sensor signal with 2 μs peaking time and perform discrimination. The binary hit information is stored in the multi event buffer that has three hit storage registers. The column readout is a hit-driven combinatorial circuit based on an asynchronous priority encoder that performs zero suppression. There is no clock propagation to the circuit and there is activity only when there is a hit.

3. Depleted MAPS

Due to the interest for applications which require extreme radiation tolerance (» 10^{13} n_{eq}/cm^2) and therefore charge collection by drift or better timing resolution (« 100 ns), MAPS with a fully depleted sensitive layer (DMAPS) are the object of intense research. Currently DMAPS are being considered for the ATLAS High Luminosity LHC (HL-LHC) upgrade and future colliders like CLIC. The ATLAS collaboration has investigated on a large number of technologies for the outer pixel layers of the Inner Tracker (ITK), which will be upgraded in 2025 for the HL-LHC [18] [19]. This section reports the sensor design concepts of the candidate technologies that are still under consideration.

3.1 Large collection electrode

In the large collection electrode designs the electronics is embedded in the n-well collection electrode that extends over a large fraction of the pixel area. Figure 3 shows a pixel cross section in the large collection electrode design.

The sensor pn junction is formed with the collection n-well and the underneath p-sub. Both NMOS transistors p-wells and PMOS transistors n-wells are nested in a shielding p-well located inside the collection electrode. This allows to decouple the PMOS bulk from the sensor input node. The large electrode sensors are implemented in High Voltage CMOS technologies (HV-CMOS) where the collection electrode can be biased at $\approx$ 100 V. This configuration creates an uniform drift field with short average distances, beneficial for radiation hardness. The sensor input capacitance is quite large (> 100 fF) in the same order of magnitude of hybrid pixels. Therefore they do not have

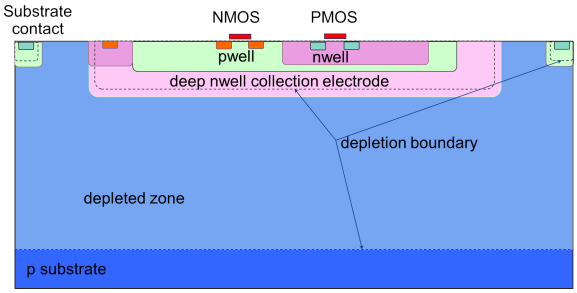

Figure 3: Cross-section of a pixel with a large collection electrode.

any advantage in terms of analog power consumption. The large sensor input capacitance is due to the large sensor junction area. In addition to that, there is a capacitance introduced by the junction between the collection n-well and the internal p-well. This p-well hosts the electronics, and the transient digital signals can couple capacitively into the sensor bulk. Therefore digital switching noise should be minimized or avoided in the in-pixel circuit. In the following two promising developments are analyzed with a highlight on their architectural choices. In both cases the sensors have been proven to be tolerant to non-ionizing radiation (10^{15} n_{eq}/cm^2), and their charge collection time is fast enough to allow a time resolution « 25 ns [20] [21].

3.1.1 ATLASpix

ATLASpix [22] is a family of large collection electrode D-MAPS implemented in AMS 180 nm HV-CMOS process. ATLASPixSimple is a prototype with a 25 $\times$ 400 pixels of 130 μm $\times$ 40 μm size for a total matrix area of 3.25 mm $\times$ 2.00 mm. The in-pixel electronics embedded in the collection n-well contains the analog circuitry for the amplification and discrimination of the sensor signal, including a 4 bit DAC for threshold adjustment (Figure 4). The absence of digital circuitry in the pixel prevent the risk of digital signal coupling into the sensor input node. The pixel matrix is trigger-less, each pixel has an output transistor that drives a digital pulse to the periphery on a dedicated line. From this pulse the periphery read-out circuit reconstructs the Time of Arrival and the Time over Threshold. This approach requires a complex routing over the pixel matrix, where the number of signal lines per column is equal to the number of rows, requiring a minimum pixel width. In this case 400 lines for a pixel width of 130 μm. On the other side the clock signal and time stamp signals are confined to a small area in the periphery, thus reducing the digital power consumption.

3.1.2 LF-Monopix

LF-Monopix is a large collection electrode D-MAPS prototype fabricated in the LFoundry 150 nm CMOS process. It has 129 $\times$ 36 pixels of 50 μm $\times$ 250 μm size for a total matrix area of 6.45 mm $\times$ 9.00 mm. The sensing volume is a high resistivity p-substrate (> 2 k$\Omega \cdot$ cm). The sensor can be thinned from the back side down to 100 μm, and reverse bias can be applied from the back side in order to achieve uniform drift field. The thinned sensor is fully depleted with a reverse bias of $\approx$ 30 V [23].

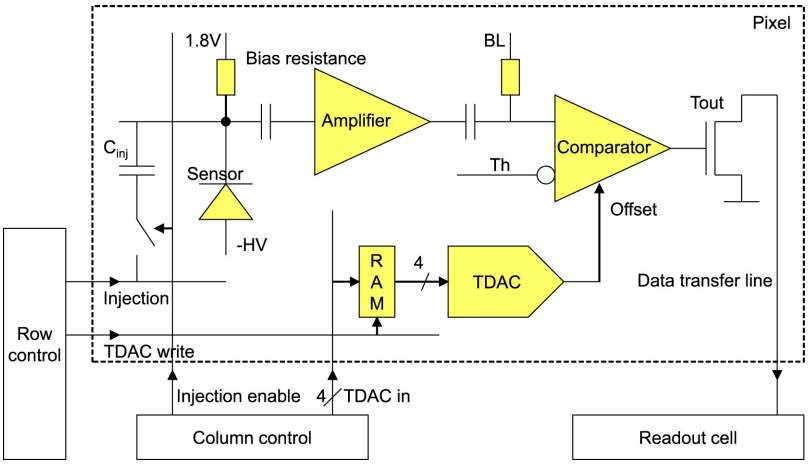

Figure 4: ATLASPixSimple pixel circuit and read-out architecture

The in-pixel circuit has a Charge Sensitive Amplifier (CSA) with a discriminator and 4 bit DAC for threshold adjustment. Due to the large sensor capacitance the static current is $\approx 20\ \mu$A/pixel to achieve a time resolution of 25 ns. The timestamp is provided from the periphery to the pixel matrix. It is used to latch the time of Arrival (ToA) and Time over Threshold (ToT) information on 8-bit RAM cells located inside the pixel. The read-out is based on the column drain architecture. It implements zero suppression with a token propagation scheme, and it presents a synchronous output to the periphery containing the pixel address, ToA and ToT information on a shared 24 bit bus at the column level (Figure 5).

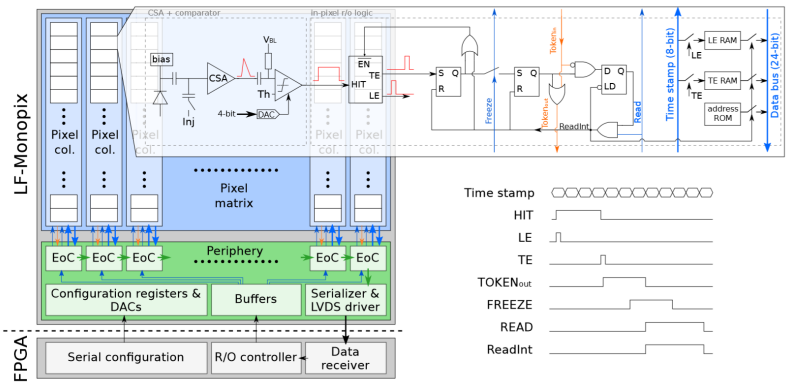

Figure 5: LF-Monopix pixel circuit and read-out based on column drain architecture.

This architecture requires the implementation of digital circuitry inside the pixel collection n-well. For this reason current steering logic is used for token propagation and the readout of the memory cells adopts a source follower as output stage, so that high current injection into the substrate of in-pixel electronics is avoided during the readout. These circuits increase the power consumption as they require static current.

3.2 Small collection electrode

In pixels with a small collection electrode, the collection electrode measures typically 2 μm or less on the side, and occupies less than 10% of the full pixel area. The electronics is in a separate well outside the collection electrode. The design is based on the TowerJazz 0.18 μm CMOS imaging process presented in Section 2.2, it allows in-pixel NMOS and PMOS transistors, as a deep-p-well shields all the other n-wells to avoid charge collection. To achieve full depletion an additional low dose blanket deep high energy n-type implant in the epitaxial layer has been introduced [16]. As shown in Figure 6 the sensor junction is between the low dose n-type implant and the p-epitaxial layer is planar. The depletion starts at the junction and with a reverse substrate bias of few V, the depletion extends to the n-well collection electrode and over the full pixel width. This allows to combine the benefits of full depletion with a small sensing node capacitance ($\approx$ 2.5 fF) that is essential for a low power pixel design and consequent material budget reduction.

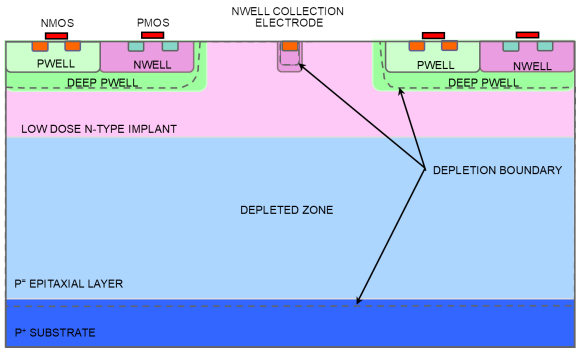

Figure 6: TJ - modified process

First measurement results on pixels with a pitch $\leq$ 30 μm [17], [29] confirm that the addition of the low dose n-type implant maintains the low sensor capacitance. The full depletion improves the timing performance and increases the non-ionizing radiation tolerance to 10^{15} n_{eq}/cm^2. For the same radiation level, pixels with a pitch $\geq$ 30 μm shows a significant signal degradation for particles incident at the pixel edges [30]. The reason is the increase of the drift time due to the very low lateral electric field at the pixel edges: the charge generated near the pixel edge gets pushed into this low field region, and it takes time for the charge to get back of this region. The two proposed solutions increase the lateral field to evacuate the charge from this region, and also shorten the drift path for carriers generated near the pixel edge. The solutions are shown in Figure 7: a) gap in the the n-layer at the pixel edges, b) additional deeper p-implant at the pixel edges.

3.3 Large scale prototypes

Two demonstrators have been prototyped in the modified TowerJazz 180 nm CMOS process to prove the small electrode design concept in a full scale system. Both demonstrators implement the same charge sensitive front-end with in-pixel discrimination which exploits the low sensor capacitance to reduce noise and analogue power. The circuit is based on the ALPIDE front-end [14] and it achieves a time resolution < 25 ns with a power consumption of 1 μW/pixel and an Equivalent Noise Charge of 7 e^-. The demonstrators implement different readout architectures,

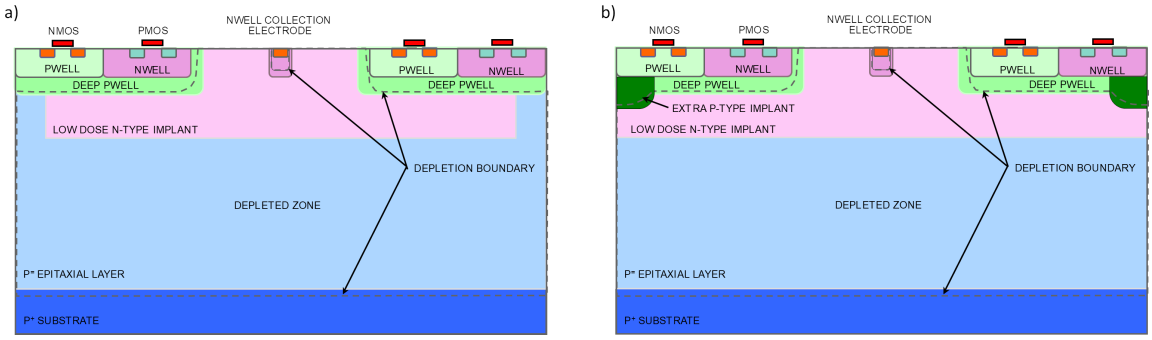

Figure 7: TJ - modified process with edge implants to increase lateral electric field

with the common requirement to cope with the expected hit rate between 0.4 and 2 MHz/mm^2. The first demonstrator is TJ-MonoPix, it is based on the column drain synchronous readout scheme. The second demonstrator is MALTA, it is based on an asynchronous readout scheme and aims to cope with higher rates with power consumption optimization.

Both prototypes have their pixel pitch larger than 30 μm and they were designed before the studies on the efficiency loss at the edges. Therefore they do not implement a solution to strengthen the lateral electric field near the pixel edges. In the following the following the architecture of the large scale prototypes is described.

3.3.1 TJ-monopix

TJ-monopix implements the Monopix column drain architecture in the small collection electrode design [27] [28]. It has 224 $\times$ 448 pixels of 36.4 μm $\times$ 40.0 μm size for a total matrix of area of 8.01 mm $\times$ 17.92 mm. The capacitance value of the small collection electrode is about 100 times lower than the large collection electrode design, this allows to reduce the pixel analog power from 20 μW/pixel to 1 μW/pixel achieving the same performance. Another benefit is that the in-pixel digital circuitry switching noise does not couple into the collection electrode. For instance the token can be propagated with compact CMOS inverters that requires switching power only, instead of the current steering logic that requires more area and static power. A 6 bit timestamp is used to latch the ToA and ToT in the in-pixel RAM cells. The pixel read-out architecture is based on the same architecture of LF-Monopix presented in Section 3.1.2.

3.3.2 MALTA

The MALTA chip implements a novel asynchronous readout scheme to reduce digital power consumption and increase the hit rate capability in the matrix. It has 512 $\times$ 512 pixels of 36.4 μm $\times$ 36.4 μm size for a total matrix area of 8.01 mm $\times$ 17.92 mm.

When the hit signal is above the discrimination threshold, the in-pixel circuit generates a digital pulse of 1 ns. This pulse is used as asynchronous reference to encode the pixel address on a 22 bits bus. The encoding system has some redundancy to reduce the probability of data collision on the bus: two busses are used for a double column (512 $\times$ 2 pixels) readout: 1 line as reference, 16 lines to locate the pixel in the sub-group of 16 pixels, and 5 lines are binary encoding the address of the 32 groups. The maximum delay for the data propagation from the pixel to the periphery is 5 ns.

This fully asynchronous readout does not require clock distribution over the matrix. This allows to save 57 mW/cm^2, the power required in this technology to propagate a 40 MHz clock over a 2 cm $\times$ 2 cm matrix. The power saving is comparable with the matrix analog power consumption of 75 mW/cm^2. In addition to that, the absence of a continuous switching CMOS signal in the matrix simplifies the design and the risk of digital to analog coupling. The digital power consumption in the matrix is proportional to the hit rate as there is only circuit activity if there are pixels hit. Table 2 shows the power consumption for the the expected pixel hit rates and the equivalent matrix readout power for the ATLAS ITk detector [31]. Presently DMAPS are a possible candidate for layer 4, in this case the asynchronous architecture makes the digital read-out power consumption negligible (2.5 mW/cm^2).

	Pixel hit rate	Power/bit/cm^2	Matrix readout power
Layer	Mhit/mm^2	mW/cm^2	mW/cm^2
0	27.2	17.7	79.6
1	8.4	5.4	24.6
2	1.72	1.1	5.0
3	1.16	0.8	3.4
4	0.84	0.5	2.5

Table 2: Matrix hit rate for ATLAS ITk layers and and readout power for a column height of 2 cm. Values for a toggling energy of 6.5 pJ/cm and average bit toggling per pixel hit of 4.5.

There are no studies to prove non-ionizing radiation tolerance for the inner layers (fluence of 10^{16} n_{eq}/cm^2). However the asynchronous architecture would allow to save 40% of the matrix digital power consumption. The matrix asynchronous bus signal can be synchronized at the end of column and read-out in the same way as it is done in synchronous architectures like Monopix.

4. Summary

Monolithic Active Pixel Sensors allow for vertex and tracking detectors with higher resolution and lower material budget, with significant advantages in term of cost and detector assembly. STAR is the first experiment to implement MAPS in 2014. ALICE will install in 2020 the ALPIDE sensor. The first MAPS to implement a zero suppression architecture to increase the read-out speed and reduce read-out power. It also fully benefits from the low sensor capacitance to reduce the analog power consumption. Fully depleted Monolithic Active Pixel Sensor (D-MAPS) are now considered for applications that require fast timing (< 25 ns) and / or larger non ionizing radiation tolerance ($\approx 10^{15}$ n_{eq}/cm^2) where the signal charge has to be collected by drift. Examples are the ATLAS High Luminosity LHC (HL-LHC) upgrade and future colliders like CLIC. Presently there are two sensors design concepts. The large collection electrode design allows full depletion and the prototypes meets both the non-ionizing radiation tolerance and the timing requirements. It suffers from a large sensor capacitance ($\approx$ 100 fF), with no benefits in term of power consumption compared with hybrid pixels. The small collection electrode design is an evolution of the ALPIDE technology. It combines full depletion with a low sensor capacitance ($\leq$ 5 fF), allowing for a power reduction. The first prototypes suffers from detection efficiency loss at the pixel edges after non-ionizing radiation. A tuning of the implants has been proposed to solve this issue, and if successful this concept has a great potential interest for the future pixel detectors.

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