Construction and quality assurance of the Belle II Silicon Vertex Detector

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The Belle II experiment, which is situated at the interaction point of the SuperKEKB e^+e^- collider at KEK, Tsukuba, Japan, is expected to collect data corresponding to an integrated luminosity of 50 ab^{-1}. This data set will be sensitive to beyond-the-standard-model physics via precision measurements and searches for very rare decays. At its heart lies a six-layer vertex detector consisting of two layers of pixel detectors (PXD) and four layers of double-sided silicon microstrip detectors (SVD). Precise vertexing as provided by this device is essential for measurements of time-dependent *CP* violation. Crucial aspects of the SVD assembly are precise alignment, as well as rigorous electrical and geometrical quality assurance. We present an overview of the construction of the SVD, including the precision gluing of SVD component modules and the wire-bonding of various electrical components. We also discuss the electrical and geometrical quality assurance tests.

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1. Introduction

The Belle II [1] experiment is a next generation flavour factory with physics goals that include, but not limited to, studies of *CP* violation in *B* and *D* meson sectors, searches for rare decays, tests of lepton flavour (universality) violation and the search for dark sector particles and forces. These physics goals are indirect probes of physics beyond the standard model. It is an upgraded version of its predecessor, Belle [2]. The Belle II detector sits at the interaction point of the SuperKEKB asymmetric e^+e^- collider [3] at KEK, Tsukuba, Japan. It is expected to collect data corresponding to an integrated luminosity of 50 ab^{-1}. The target peak luminosity of SuperKEKB is 8×10^{35} cm^{-2}s^{-1}. The beam current will be twice and beam size $\frac{1}{20}$ as that of KEKB.

The inner tracking system consists of two layers of DEPFET based pixel detectors (PXD) and a four layer silicon vertex detector (SVD), which consists of double-sided silicon microstrip sensors. This improves the vertex resolution significantly compared to Belle, which is crucial for measurements of time-dependent *CP* violation. The impact parameter resolution is 20 μm at 2 GeV/*c* [1], which is almost half that of Belle. The reconstruction efficiency of low momentum particles and relatively long-lived particles like K_S^0 will be improved due to the larger radius of the outermost SVD layer. The physics run with the full detector, except for one layer of PXD, is expected to start in early 2019.

2. Belle II Silicon Vertex Detector

The Belle II SVD has four layers and its construction is a global effort involving groups from Asia, Australia and Europe. Layer 3 (L3) is constructed by a research group at the University of Melbourne. Layers 4, 5 and 6 (L4, L5 and L6) are built by TIFR India, HEPHY Vienna and Kavli IPMU Japan, respectively. The forward and backward modules for L4, L5 and L6 are provided by INFN Pisa.
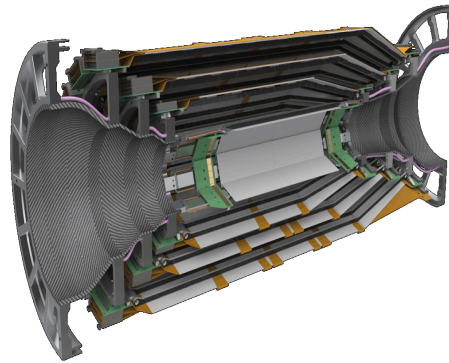
Figure 1: A cross-section view of the Belle II SVD.

A cross-section view of the SVD is shown in Fig. 1. L3, L4, L5 and L6 are made up of seven, 10, 12 and 16 modules (also referred to as "ladders"), respectively. The angular acceptance is $17° < \theta < 150°$. The innermost layer (L3) has a radius of 39 mm and the outermost one (L6) is 135 mm in radius. The radii for L4 and L5 are 80 mm and 104 mm, respectively. In comparison,

Sensor	Rectangular (large)	Rectangular (small)	Trapezoidal
# of p-strips	768	768	768
p-strip pitch (μm)	75	50	50–75
# of n-strips	512	768	512
n-strip pitch (μm)	240	160	240

Table 1: DSSD specifications used in SVD.

the radius of the outermost SVD layer at Belle was 88 mm [4]. The whole structure has a lantern shape to complement the forward boost of the centre of mass system because of the asymmetric beam energies (4 GeV e^+ and 7 GeV e^-). To facilitate this, L4, L5 and L6 have slant angles of 11.9°, 17.2° and 21.1°, respectively. This structure reduces the material budget without affecting the performance.

3. Components used for SVD

Three types of double-sided silicon microstrip detectors (DSSD), which are p-in-n type, are used to build the ladders of the SVD. They are six inches long with differing width and have thickness 300 or 320 μm. The small rectangular DSSDs are used in L3 whereas large rectangular ones are used in L4, L5 and L6. The forward slanted part is built using trapezoidal DSSDs with varying width. The DSSDs are shown in Fig. 2 and their specifications are given in table 1.
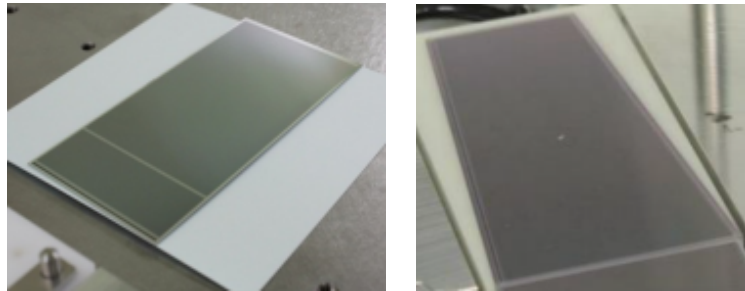

Figure 2: Rectangular (left) and trapezoidal (right) sensors.

The p-side strips are aligned parallel to the beam direction and n-side strips are perpendicular to the beam direction. The L3 DSSDs have their n-side facing the beam pipe whereas L4, L5 and L6 DSSDs are oppositely arranged. This design avoids any interference of L3 support structure with the PXD system. The rectangular DSSDs are manufactured at Hamamatsu Photonics in Japan and the trapezoidal DSSDs are built at Micron Semiconductor in the UK.

The readout chip must have a short signal shaping time in order to cope with the high hit rate expected at Belle II. The APV25 chips [5], originally developed for the CMS Collaboration, is used

for this purpose, which has an integration time of 50 ns. It is radiation hard and can tolerate upto 1 MGy, which is far beyond the radiation dose expected at Belle II (about 50 Gy). It also has a 192 cell deep analog pipeline, which reduces the detector dead-time. The chip is shown in Fig. 3.
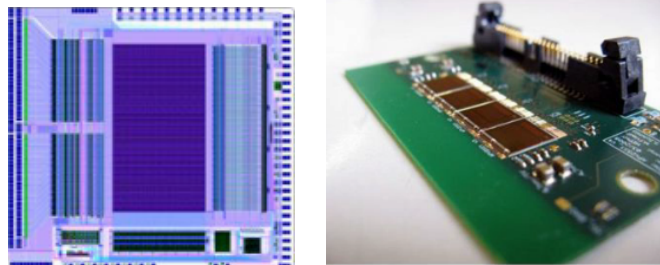
Figure 3: Image of the APV25 readout chip showing the features and bond pads (left); four APV25 readout chips mounted on a hybrid (right).

The APV25 needs to be placed as close to the DSSD as possible to reduce the capacitive noise. This is done with the "origami" chip-on-sensor concept [6]. This novel design allows for the readout chips to be on a single side of the DSSD. The readout channels from the other side are wrapped around via flexible electronic circuits so that the APV25 chips can be placed on a single line (see Fig. 4). This, in turn, helps in having a single cooling channel, thus reducing the material budget. This origami concept is adopted in the inner DSSDs of L4, L5 and L6. The full L3 ladder and the forward and backward DSSDs are read out from the edges.
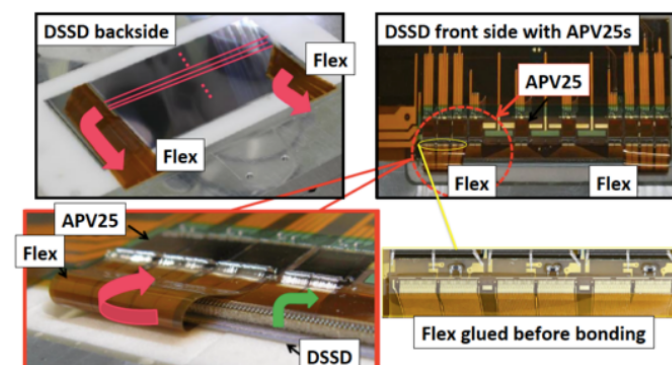

Figure 4: Origami chip-on-sensor concept where the readout from the other side of the DSSD is wrapped around using flexible circuits and connected to APV25 chips in a single line on the DSSD.

A dual-phase CO_2 cooling system at $-20°C$ is employed to deal with the heat dissipated, approximately 700 W, from all the APV25 chips.

4. Construction

The ladder assembly procedure [7] is complex because the DSSDs are aligned precisely using assembly jigs. Vacuum chucking is used to fix the sensors to the jigs. There are different jigs used for various purposes during the entire assembly of one ladder. The flexible circuits are glued to sensor and the electrical connections are made via wire-bonding. Araldite® 2011 glue is used and

the dispensing is controlled by robotic arm. A uniform glue thickness is achieved with the robotic system as demonstrated in Fig. 5.
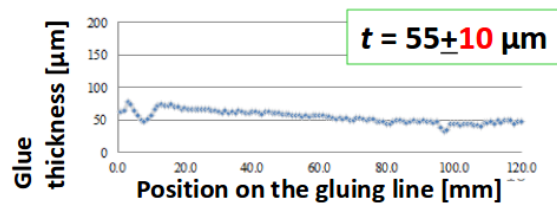

Figure 5: Thickness of the glue dispensed by the robotic arm.

The wire-bonding machine uses Aluminuim wire for the connections. The machine parameters are fine tuned to realize a yield $> 99\%$ and pull strength f such that the mean $\mu_f > 5$g and $\frac{\sigma_f}{f} < 20\%$, where σ_f is the standard deviation in f, as shown in Fig. 6.
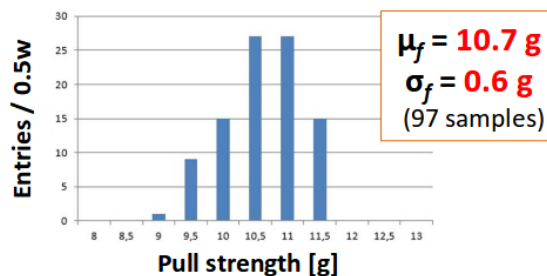
Figure 6: Pull strength measured for 97 samples of wire-bonds.

Thermally insulating Airex sheets (light-weight styrofoam) are placed between the DSSD and the readout circuits to minimize the heat transfer between them. This also provides electrical isolation and hence avoids the signal cross-talk. The APV25 chips on the origami flexible circuits are thinned down to 100 μm to further reduce the material budget. Each ladder is supported by ribs built from carbon-fiber reinforced Airex foam, which is very light but strong and stiff. A completed L4 ladder is shown in Fig. 7.
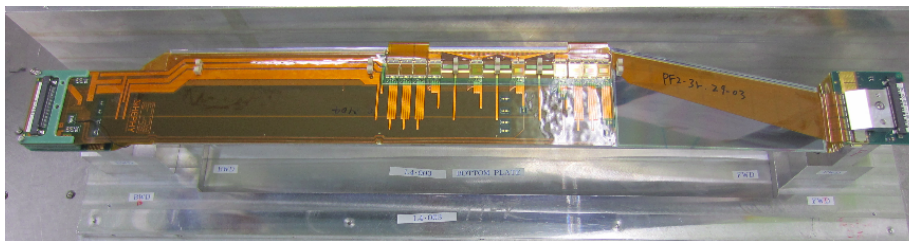

Figure 7: A completed layer 4 ladder.

A major challenge during the mass production was that the glue joint between the flexible circuit and the forward DSSD was found to be lifting off on some L4 and L6 ladders. The likely cause was the small overlap between the sensor and the circuit and the stress due to the bending angle. A glue reinforcement strategy is implemented to tackle this issue.

5. Quality assurance

The geometrical and electrical quality of the produced ladders are rigorously tested at the assembly sites as well as at KEK, where the ladders are mounted to the support structure. The geometrical precision is measured with an optical Coordinate Measuring Machine (CMM). The position of each sensor is measured and the deviations from the designed values are calculated. The coordinate system used is shown in Fig. 8.
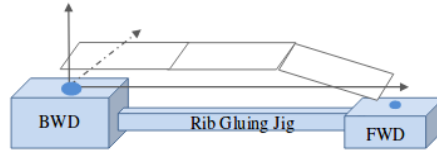
Figure 8: Ladder coordinate frame for L4.

Deviation upto 150 μm in the x-y plane and 200 μm along the z axis are allowed. The deviations are found to be within the tolerance limits for all the ladders in all the layers. An example of CMM results for an L4 ladder is given in table 2.

|	FW	CE	BW
Δx (μm)	-44	6	-47
Δy (μm)	25	-21	-9
Δz (μm)	174	-139	-81
slant angle (°)	-11.91	-0.07	-0.03
tilt angle (°)	0.09	0.09	0.02

Table 2: Typical CMM results for an L4 ladder. FW, CE and BW stands for forward, central and backward DSSDs.

Electrical quality of the connections between the sensor and the readout chips is tested. Electrical signals are randomly triggered to evaluate noise, raw noise and the pedestal for each channel. The I-V characteristics of each sensor are analysed and a typical plot is given in Fig. 9. A source scan is performed using a β source (^{90}Sr). All ladders have been tested to have good electrical response.

A module with one ladder from each layer was tested at DESY beam line in April 2016 [8]. Excellent strip hit efficiency of $> 99\%$ was obtained. This module is also tested during the pilot run of Belle II during April–July 2018. The obtained signal to noise ratio and hit time resolutions are in agreement with the Monte Carlo expectations. All the SVD ladders have been mounted to the final structure successfully and an event display of the first track, induced by a cosmic ray muon, is shown in Fig 10.

6. Conclusions

The SVD plays a crucial role in Belle II obtaining its physics goals by providing excellent spatial resolution. The assembly procedure for the ladder modules has been established after rigorous
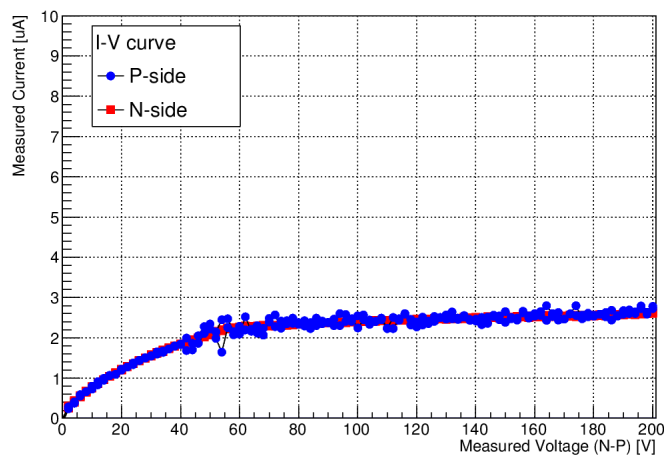
Figure 9: I-V characteristics for an L4 DSSD.
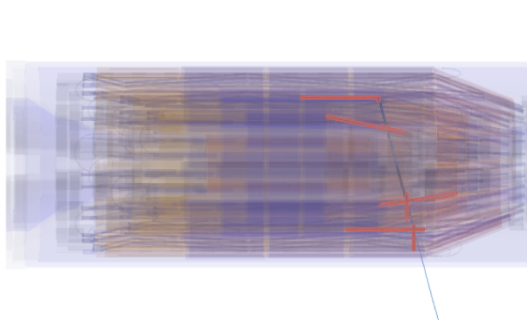
Figure 10: First cosmic track seen in the full SVD on July 17, 2018.

research. All the ladders have been produced with good electrical and mechanical quality. They have been mounted to the final structures and are ready for the first Physics run, which is expected to kick-off in early 2019.

Acknowledgments

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