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Upgrade of the ATLAS Thin Gap Chamber Electronics for HL-LHC runs

Haruka Asada*
on behalf of the ATLAS Muon Collaboration

Nagoya University
E-mail: asada@hepl.phys.nagoya-u.ac.jp

The High-Luminosity LHC (HL-LHC) is planned to start the operation in 2026 with an instantaneous luminosity of 7.5×10^{34} cm^{-2}s^{-1}. In order to cope with higher proton-proton collision rate, the trigger and readout electronics of ATLAS Thin Gap Chamber (TGC) needs to be replaced. All hit data will be transferred from the frontend to the backend boards, and a fast-tracking algorithm will be applied on these hits for the first-level muon triggering. The first prototype of the frontend board has been developed with full functions required for HL-LHC runs including the data transfer of 256 channels with a 16 Gbps bandwidth and the control of the discriminator threshold. They were demonstrated at the CERN SPS beam facility. The rate of single event upsets in Kintex-7 FPGA integrated on the prototype board was measured in the ATLAS detector area, and automatic error correction was demonstrated. The fast-tracking algorithm was performed using a Monte-Carlo sample and data taken by ATLAS. The result indicates that the advanced trigger based on fast-tracking reduces the trigger rate by 30% while increasing the efficiency by a few percent. These studies provide essential ingredients in the development of ATLAS TGC electronics for HL-LHC.

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*Speaker.

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1. Introduction

Upgrade of Thin Gap Chamber (TGC) electronics is essential for the ATLAS experiment [1] at the High-Luminosity LHC (HL-LHC) [2]. HL-LHC is planned to start in 2026 after the Long Shutdown 3. The instantaneous luminosity will ultimately increase to 7.5×10^{34} cm^{-2}s^{-1}, and after ten years of operation, 3000 fb^{-1} of data will be delivered for precise measurements of the Standard Model and searches for new physics. To cope with higher instantaneous luminosity and maximize the discovery potentials at the HL-LHC, the trigger and readout electronics of TGC need to be replaced. In this document, the overview of TGC electronics for HL-LHC and the status of the development are reported.

2. TGC electronics for HL-LHC

We plan to replace most of the electronics of TGC except for amplifier-shaper-discriminator (ASD) boards in 2024–2026 [3]. The block diagram of TGC electronics for HL-LHC is shown in Figure 1. TGC is a multi-wire proportional chamber in the endcap middle station of the ATLAS muon spectrometer and covers a pseudorapidity range ($|\eta|$) of 1.05–2.4 [4]. Two-dimensional positions of muons are provided by TGC using signals from wires and strips. TGC consists of three stations. The station M1 has three layers. Each of the stations M2 and M3 has two layers. The PS boards receive the signals from ASD boards, perform time alignment, and transfer the data to the off-detector electronics with a transfer rate of 16 Gbps per board. The PS boards also control the threshold of the ASD boards. The Endcap Sector Logic (SL) boards receive the signals from PS boards. Each Endcap SL board has one FPGA for data readout and trigger processing.

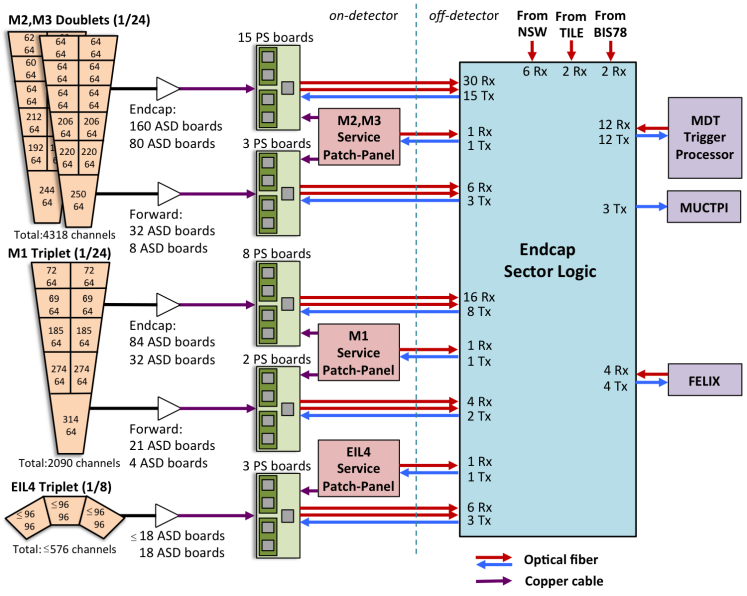

Figure 1: Schematic diagram of TGC electronics covering 1/24 of one side of the endcap region for HL-LHC. The two numbers in each box describing a TGC chamber show the number of channels of wire (top) and the number of channels of strip (bottom), respectively.

The current first-level endcap muon trigger employs simple coincidence logic in the on-detector boards to identify the muon track candidates and transverse momentum (p_{T}) evaluation with look-up tables in the off-detector boards. The new trigger for HL-LHC is based on the fast-tracking algorithm. All TGC hits are transferred from the PS boards to the Endcap SL and used for TGC track segment reconstruction. The trigger evaluates p_{T} in Endcap SL from the angle difference between segments reconstructed by New Small Wheel (NSW) [5] and TGC.

3. Demonstration with PS board prototype

3.1 Full TGC readout chain

A beam test was performed with charged particle beams at SPS H8 beamline in CERN to confirm the functions for the hit data transfer and the threshold control of an FPGA of PS board prototype. The prototype has full functions required for HL-LHC implemented. Figure 2 (left) shows the setup. Hit data from TGC are sent to PS board prototype. PS board prototype transfers the data to Endcap SL prototype for Run-3.

The result shows that PS board prototype provided stable data transfer for two weeks of the test period. The validity of the transferred data was confirmed by evaluating the efficiency for each channel shown in Figure 2 (right). The efficiency is found to be close to 100% except for the channels near the support structures. The threshold control based on FPGA was also demonstrated and confirmed.

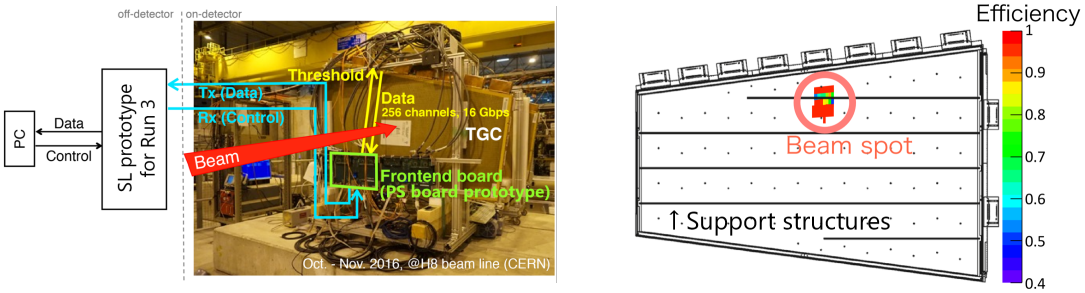

Figure 2: Left: The setup of the beam test at H8 beamline. The charged particle beam is irradiated to TGC. Its hit data are transferred from PS board prototype to Endcap SL prototype. Right: The efficiency measured in the beam test [6]. The pink circle shows the beam spot. The black lines and dots in the chamber indicate support structures.

3.2 Soft Error Mitigation

A test of Soft Error Mitigation (SEM) system of a Xilinx Kintex-7 FPGA on PS board prototype was performed in the ATLAS detector area. A PS board prototype was installed on the top of TGC about 13 m away from the beam axis. The expected particle rate in this area is smaller than the actual PS board area by a factor of two. The setup is shown in Figure 3. The SEM controller [7] monitors the data stored in the configuration memory. The status of the SEM controller and the count of Single Event Upsets (SEUs) are monitored via Endcap SL prototype for Run-3. The SEM demonstration was performed for about nine weeks.

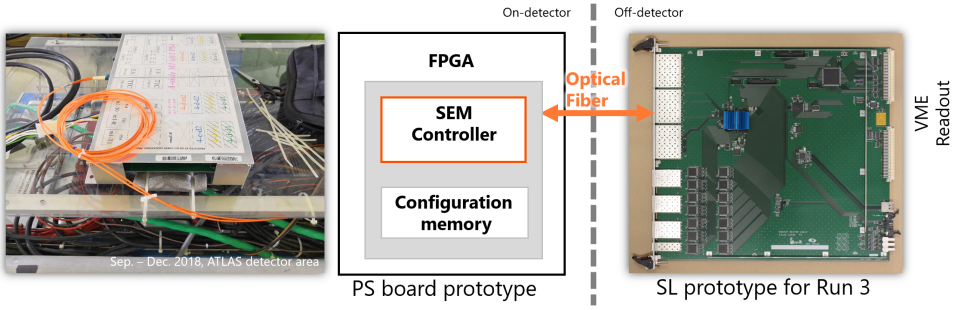

Figure 3: The setup of the SEM demonstration. The SEM controller is implemented on the Kintex-7 FPGA of PS board prototype. PS board prototype communicates with Endcap SL prototype via optical fibers.

As a result, 16 SEUs were found on one FPGA of PS board prototype during the period that 12.6 fb^{-1} of data were taken. Figure 4 shows the cumulative count of SEUs as a function of the integrated luminosity. All SEUs were one bit errors and were automatically corrected by the SEM controller. No communication error was observed during the demonstration.

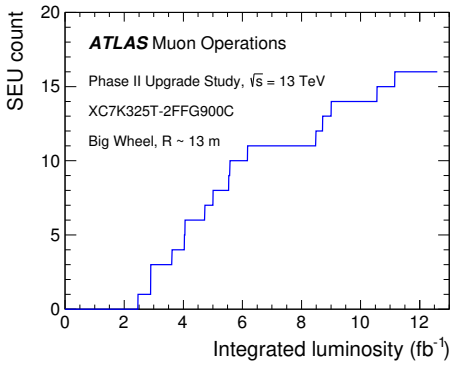

Figure 4: The SEU count in Kintex-7 FPGA of PS board prototype depending on the integrated luminosity.

4. TGC segment reconstruction

The fast-tracking trigger performance for HL-LHC was evaluated. The triggering algorithm includes TGC segment reconstruction with pattern matching. The efficiency of TGC trigger was studied with a Monte-Carlo sample having one muon track per event. Figure 5 (left) shows the trigger efficiency as a function of the offline muon p_{T} for a p_{T} threshold of 20 GeV. HL-LHC scheme shows higher efficiency by a few percent in plateau than that of Run-1 scheme. The rate for the first-level single muon trigger in the endcap region for 15 GeV and 20 GeV thresholds were estimated using data taken by ATLAS. The result is shown in Figure 5 (right). The total rate of muon candidates from the Endcap SL for 20 GeV threshold is less than 30 kHz for the expected luminosity at the HL-LHC.

5. Conclusion

The development of the ATLAS TGC electronics for HL-LHC is ongoing. The prototype of PS

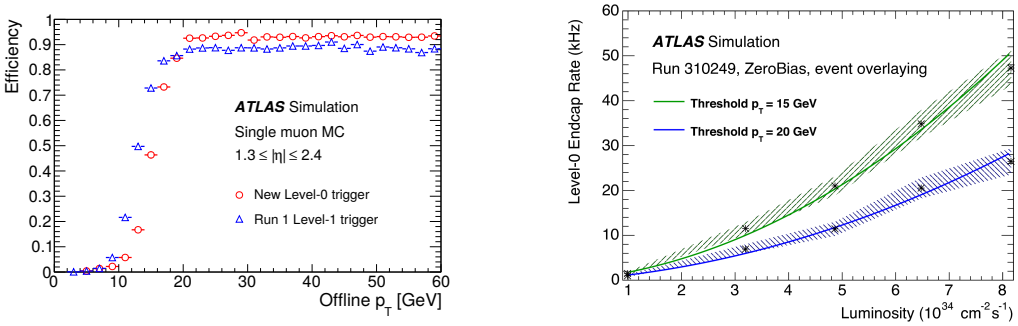

Figure 5: Left: The estimated efficiency of the first-level muon trigger for 20 GeV threshold in the region $1.3 \leq |\eta| \leq 2.4$ based on TGC and NSW [8]. Red and blue plots show the HL-LHC scheme and Run-1 scheme, respectively. Right: The estimated rate of the first-level single muon trigger for $1.05 \leq |\eta| \leq 2.4$ based on TGC, Tile calorimeter, and NSW [8]. The curves show the fitting result by a quadratic function.

board was used to demonstrate TGC full readout chain and SEM technique. In the demonstration at SPS H8 beamline, PS board prototype transferred TGC hit data stably for two weeks. The SEM test was performed in the ATLAS cavern. Sixteen SEUs were observed and were corrected automatically by the SEM controller implemented in the FPGA. The first-level endcap muon trigger for HL-LHC is based on a fast-tracking algorithm. The efficiency and the rate of the new trigger with TGC segment reconstruction by pattern matching have been evaluated. The trigger for a p_{T} threshold of 20 GeV shows higher efficiency than Run-1 scheme. The rate of muon candidates from the Endcap SL for 20 GeV threshold is estimated to be less than 30 kHz for an instantaneous luminosity of 7.5×10^{34} cm^{-2}s^{-1}.

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