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Development of the muon tracking trigger based on Thin Gap Chamber for the ATLAS experiment at High-Luminosity LHC

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The ATLAS trigger system is essential to efficiently select the events of high interest for physics analyses. Development of a new muon trigger is ongoing for High-Luminosity LHC, which is scheduled to start in 2026. The first stage of the new trigger system assumes muon track reconstruction from Thin Gap Chamber (TGC) hits with an angular resolution of 4 mrad. An algorithm with pattern matching for a pseudorapidity range of 2.13–2.16 was implemented in an XCVU9P FPGA and demonstrated with test samples including seven hits on seven TGC layers. The implemented algorithm reconstructed tracks successfully with an angular resolution of less than 4 mrad. In addition, GTY transceiver on XCVU9P FPGA was tested. Measured bit error ratio was less than 2.5×10^{-16}, and the power consumption for 100 pairs of transmitters and receivers was estimated to be about 30 W.

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1. Introduction

High-Luminosity LHC (HL-LHC) is planned to start in 2026 for precise measurements of the standard model and direct searches for new physics [1]. HL-LHC ultimately reaches a peak instantaneous luminosity of 7.5×10^{34} cm^{-2}s^{-1} and provides a total integrated luminosity of 4000 fb^{-1}, which is more than ten times of the assumed total integrated luminosity of the LHC runs. However, a higher instantaneous luminosity increases the background rate. To suppress the background, the trigger system in the ATLAS experiment [2] needs to be upgraded. In this report, an overview and the status of hardware development are presented for the first-level muon trigger system in the endcap regions.

2. First-level endcap muon trigger for HL-LHC

First-level endcap muon trigger for HL-LHC employs the fast-tracking algorithm as shown in Figure 1 [3, 4]. In addition to New Small Wheel (NSW) [5], which is scheduled to be introduced in 2019–2020, Thin Gap Chamber (TGC) provides the muon segments. TGC is the muon detector located after the endcap toroid magnet. It consists of three stations. The station M1 has three layers. The stations M2 and M3 have two layers, respectively. Frontend boards of TGC send all hit signals to backend boards, in which muon segments are reconstructed. It allows evaluation of transverse momentum (p_{T}) from the angle difference between NSW and TGC segments β. Previous study showed that the tracking trigger increases the trigger efficiency by a few per cents and reduces the trigger rate [4].

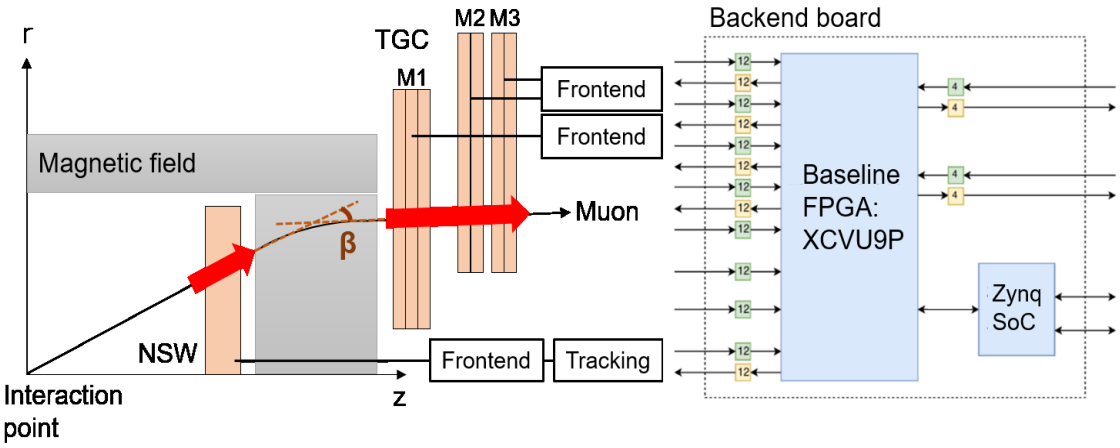

Figure 1: The concept of the tracking trigger algorithm for HL-LHC. The z-axis is along the beam pipe, and the r-axis is perpendicular to the pipe. Frontend boards of TGC send all hit signals to backend boards, in which muon segments are reconstructed. Bold arrows indicate reconstructed muon segments. The numbers in green boxes are the numbers of receivers and those in yellow boxes are the numbers of transmitters, respectively.

TGC segments are reconstructed with pattern matching on an FPGA mounted on the backend board. The angle and the position of a segment are extracted from a predefined list of TGC channels

and segments. A preliminary estimate on the memory size required for the predefined list per backend board is 120 Mb. The FPGA is required to have a memory resource with a larger size. The FPGA is also required to have 104 receivers and 68 transmitters for receiving and sending a huge amount of hit and control signals. The assumed transfer rate is 6.4–9.6 Gbps depending on the links. The majority of the receivers is used for the receipt of hit signals of about ten thousand TGC channels. For meeting these requirements, Virtex UltraScale+ FPGA provided by Xilinx [6], XCVU9P, is assumed to be implemented on the backend board.

3. Demonstration of TGC segment reconstruction

TGC segment reconstruction algorithm was demonstrated for limited hit patterns in a small detector coverage with XCVU9P FPGA with UltraRAM [7]. The test firmware was implemented on VCU118 evaluation board [8].

A two-step algorithm of TGC segment reconstruction is under study. The first step is the station coincidence. In this step, coincidence for each of the M1, M2, and M3 stations is taken and the incident position of the muon in each station is obtained. The second step is the segment extraction. The position and the angle of the segment are extracted from the predefined list of TGC channels and segments by using the incident position for each station. We aim to reconstruct the TGC segments with an angular resolution of 4 mrad or better.

The firmware to reconstruct segments from seven hits in pseudorapidity η range 2.13–2.16 was developed. Input data is 100 event samples of TGC hits with an assumed p_{T} of 20 GeV. Each event is required to have exactly seven hits on the seven TGC layers. As a result, segments were reconstructed successfully for all events. Figure 2 shows the angular distribution of reconstructed segments. The mean is 0.3 ± 0.2 mrad and the RMS is 2.0 ± 0.1 mrad. The obtained resolution is less than 4 mrad.

4. Demonstration of GTY transceiver

GTY transceiver [9] on XCVU9P FPGA was tested with loopback using IBERT [10]. Figere 3 shows the setup. A pattern generator in IBERT transmits 31-bit pseudo-random binary sequence (PRBS) to QSFP28 module on the VCU118 evaluation board. PRBS signals are transferred through loopback module with copper paths and checked at a pattern checker inside the FPGA. The bit error ratio (BER) and the power consumption of FPGA are evaluated.

BER was measured by comparing the data detected by the normal clock and the data detected by the clock with offset. The Statistical Eye [9] for a transfer rate of 10 Gbps is shown in Figure 4. The horizontal axis shows the timing offset, and the vertical one the voltage offset. A large open area was obtained. At zero offsets, no bit error is measured and BER is less than 2.5×10^{-16}. This value indicates that less than one bit error occurs for receipt of TGC signals in about ten million proton-proton collisions.

The Xilinx Vivado design tool [11] was used to evaluate the power consumption of transceivers in XCVU9P. The power consumption per FPGA on the backend board was estimated to be about 30 W. This is sufficiently smaller than an ATLAS requirement on one ATCA blade of 400 W [4].

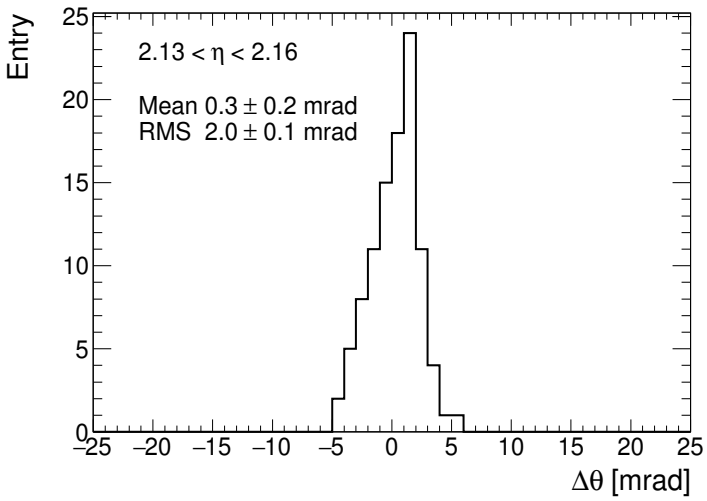

Figure 2: The distribution of the angular difference $\Delta\theta$ between the TGC track segment reconstructed by the two-step pattern matching in XCVU9P FPGA and the truth segment. Samples used in the test are provided assuming $p_{\mathrm{T}} = 20$ GeV, $2.13 < \eta < 2.16$, and one hit for each layer in straight line.

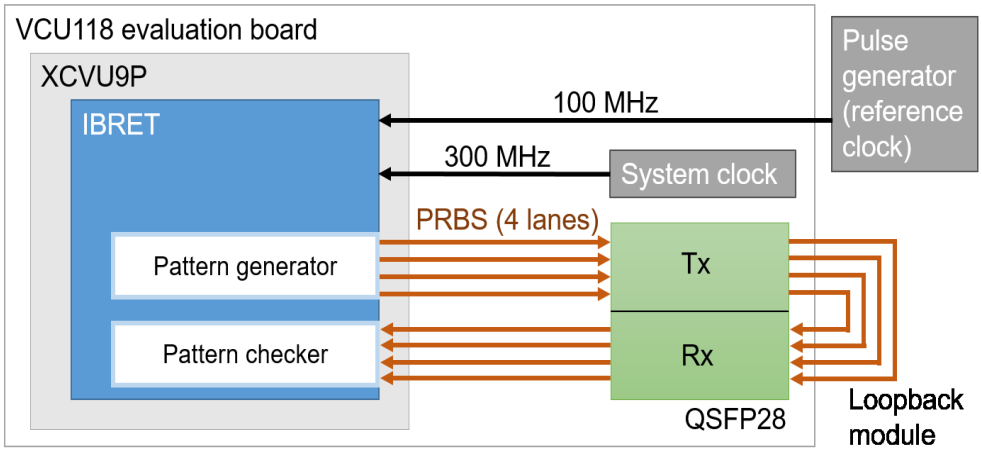

Figure 3: The block diagram of the loopback test on the VCU118 evaluation board. Black and red arrows indicate the paths of clock signals and PRBS signals, respectively. Reference clock for GTY transceiver is provided from an external pulse generator.

5. Conclusion

The development of a new muon trigger system for HL-LHC is ongoing. The new first-level muon trigger for endcaps is based on a fast-tracking algorithm and expected to improve p_{T} resolution and suppress the backgrounds. Firmware of TGC segment reconstruction with a two-step pattern matching algorithm was implemented on XCVU9P FPGA and demonstrated with test samples. The result showed an angular resolution of less than 4 mrad. GTY transceiver on XCVU9P

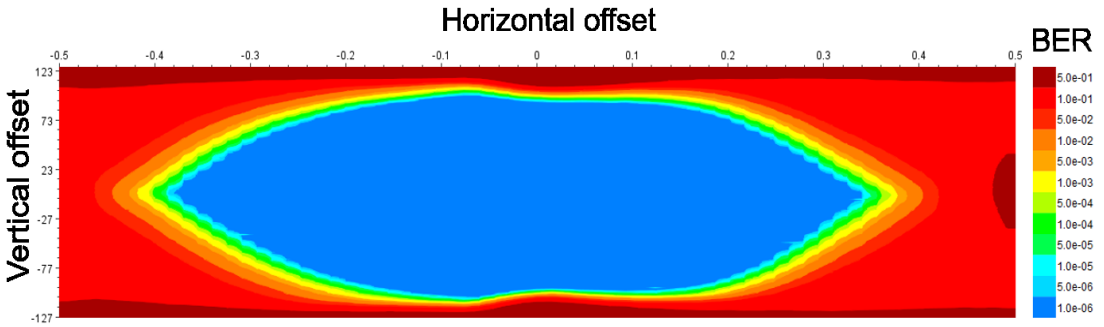

Figure 4: Statistical Eye measured by IBERT for XCVU9P FPGA with 10 Gbps. The horizontal axis shows the timing offset and the vertical one shows the offset of the differential voltage.

FPGA shows high performance of serial data transfer and measured BER was less than 2.5×10^{-16}. The power consumption for 100 transceivers in the FPGA on the backend board was estimated to be about 30 W, which is less than an ATLAS requirement on an ATCA blade. These results constitute essential ingredients in the development of first-level endcap muon trigger for HL-LHC.

References

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