Design of an FPGA Based TDC Readout Electronics for Prototype Mars Ion and Neutral Particle Analyzer

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Abstract: In order to understand the escape of the Martian atmosphere, study the interaction between the solar wind and the Martian atmosphere, and research the acceleration mechanism of neutral particles near the Martian shock, the characteristics of particles in Mars plasma will be explored. A Mars ion and neutral particle analyzer prototype having three functions: Energy analysis, direction analysis and composition analysis, has been developed. A mass spectrometer using Time-of-Flight (TOF) structure based on ultra-thin carbon film, which can obtain a high resolution, has been used to implement composition analysis. Because temperature varies greatly on Mars, in order to distinguish TOF of different particles, the TOF system requires a time resolution of less than 600 ps within the temperature range of -40°C to +60°C. In this paper, a prototype electronics mainly including a time-to-digital converter (TDC) implemented in Field Programmable Gate Array (FPGA) for mass spectrometer is described. For anti-irradiation considerations, the TDC architecture is implemented in a flash FPGA, and adopted Triple Module Redundancy (TMR) to mitigate Single-Event-Upset (SEU). Online correction is adopted to ensure that TDC can work accurately in the large temperature range. Rom-temperature's test results show that a time resolution of 539ps with a 239 ps RMS was obtained. Thermal tests suggested that the prototype electronics operates well in a temperature range from -40°C to +60°C with an RMS less than 305.5 ps.

Key words: Time-of-flight, TDC, Temperature online correction, Mass spectrometer

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1. Introduction

In the course of Mars exploration, the detection of the Martian space environment is usually the vanguard. For the purpose of understanding the evolutionary of Mars, targeted detection and research should be carried out, to explore the Martian space environment. Mars space includes charged particles, neutral particles, electric field, magnetic field, etc. Ions and neutral particles are important groups in the Martian space, which are the important goals of the previous Mars space detection. To research the atmospheric ionosphere and surface climate and environment of Mars, an ion and neutral particle analyzer prototype, mainly aimed at exploring the characteristics of particles in Mars plasma, understanding the escape of the Martian atmosphere, studying the interaction between the solar wind and the Martian atmosphere and acceleration mechanism of neutral particles near the Martian shock, has been developed.

In order to accomplish these tasks, the prototype used top-hat electrostatic analyzer scheme has been developed [1]. The instrumentation owns three functions: energy, direction and composition analysis. The diagram of analyzer is given in Fig.1. A mass spectrometer uses TOF structure based on ultra-thin carbon film is applied, which has been used to implement composition analysis.
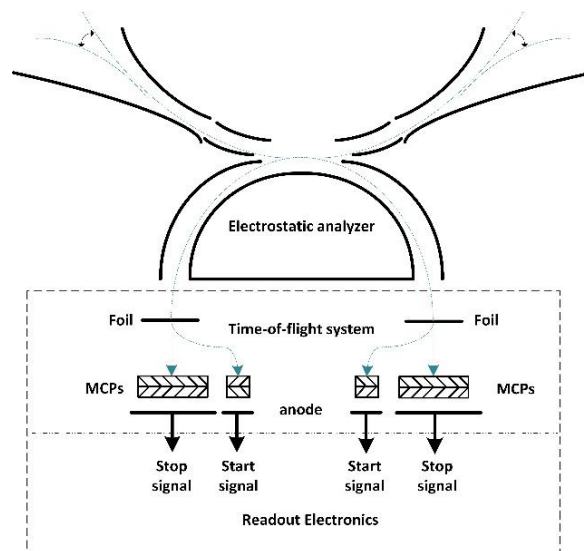

Fig.1 Diagram of the TOF composition analyzer

The electrostatic analyzer screens out the targeted ions according to their energy per charge (E/Q). Subsequently, the ions are accelerated by a fixed acceleration voltage U_{ACC} (>15 kV). The ions entering the TOF system first pass through the carbon film and loses part of energy while producing secondary electrons, deflecting by the deflection electrode in the TOF system onto the starting micro-channel plate (MCP), producing a start signal. The ions passing through the carbon film continue to fly for a distance in the TOF system and hit the terminating MCP, producing a stop signal. The start and stop signals enter the readout electronics system, which are processed by the readout electronics to obtain the time of flight. There are two channels in mass spectrometer, therefore, the readout electronics is also designed to have two channels.

In this paper, a design of readout electronics based on high-resolution time measurement with large temperature range for a TOF mass spectrometer applied in Mars orbit is reported.

2. Electronics implementation

The TOF mass spectrometer is the most common and effective method for low-energy ions analysis. This method has a high resolution of mass spectrometry and was used in interplanetary missions frequently, such as Observatory Mission PLASTIC and MAVEN STATIC. The emphasis of the TOF approach is to measure the flight time of ions over a fixed flight distance. The time of flight is given by measuring the time difference between the start signal at the begin of the flight distance and the end signal at the end. The mass per charge (M/Q) of the ions is determined by Eq. (1)

$$M/Q = 2(E/Q + eU_{ACC} - E_{loss})/(d/\tau)^2$$

E/Q is determined by the electrostatic analyzer; U_{ACC} is the acceleration voltage; d is the length of the TOF region; τ is the flight time of the ions; E_{loss} is the energy lost by ions passing through thin carbon foil. As a result, it is essential to measure the flight time accurately. According to atmospheric composition of Mars, the main particles that the prototype aims to distinguish are O_2^+ and CO_2^+, etc. So that time resolution less than 600ps and large dynamic range are demanded by TOF system [2]. In addition, in order to improve the event rate of mass spectrometer, low dead time was required. TDCs with different principles have been used for the time measurement for many space programs. For instance, in STATIC of MAVEN mission, discrete-component TDC was applied, whose disadvantage is low integration [1]. The TDC-GP1 (ASIC made by ACAM company) was adopted to measure time in the LTT experiment, which had a fine time resolution but its large dead time is not suitable for the TOF system [3]. The TDC based on FPGA can provide higher integration and smaller dead time. In the COSIMA of the ESA mission Rosetta, TDC was implemented in FPGA from ACTEL, which used time interpolation technique and utilized CMOS buffer as delay unit, obtaining a time resolution about 1.95 ns that is not up to demand [4]. Smaller delay unit of the FPGA-TDC reaches higher time resolution. Compared with techniques already used in former interplanetary missions, logic gate has been proved to be more suitable as delay unit. In view of this, an improved TDC based on FPGA combining time interpolation technique is adopted, which can get less than 600 ps time resolution and programmable dynamic range. Besides, multiple channels can be integrated on single FPGA, achieving higher integration, which is more suitable for interplanetary missions. Benefiting from pipeline process of the FPGA, dead time of FPGA-TDC is small. In addition, target of the prototype is to work in Mars orbit, which requires that readout electronics works normally in the temperature range of -40°C to +60°C, referring to the large temperature variations environment on Mars.
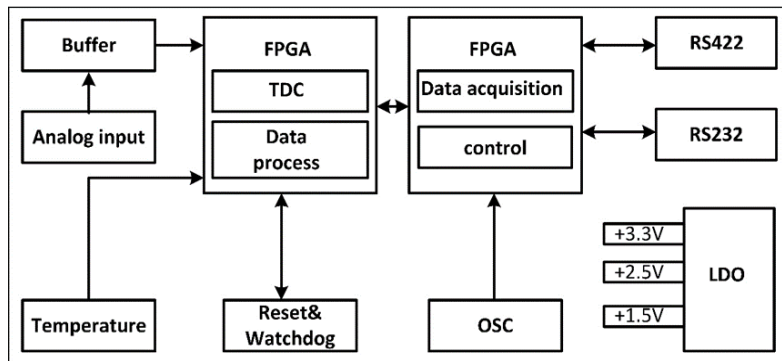

Fig2 Diagram of the readout electronics

As shown in Fig.2, the readout electronics is mainly composed of two FPGAs (one built-in TDC and the other for data acquisition and control), power module (LDO), and interface module

(RS422 and RS232). The analog signals first pass through buffer and then enter the FPGA-TDC. The ambient temperature is measured by two dedicated chip (DS18S20Z). The function of Reset & Watchdog module is to confirm that the whole system is working normally. The focus of the whole readout electronics is on the TDC structure and online Correction method.

2.1 TDC structure

The readout electronics uses a time-to-digital convert method called time interpolation technique based on FPGA. The basic idea of time interpolation technique is to subdivide the reference clock cycle of the system into N equal parts so that higher time resolution can be obtained [5]. Time measurement is divided into two parts: coarse time and fine time. Considering the requirement of low-power consumption in interplanetary missions, flash FPGA (APA600) is chosen. There are four independent channels of TDC, which can process two pairs of start and stop signals. As shown in Fig.3, each channel has a configurable 4-bit counter, following by a 4-bit register to record the counter value when event signals rise. In order to reach higher resolution, the delay time of each delay unit is expected to be as small as possible. As a result, OR3 is selected with the smallest delay in common logic gates by simulation with Microsemi software.
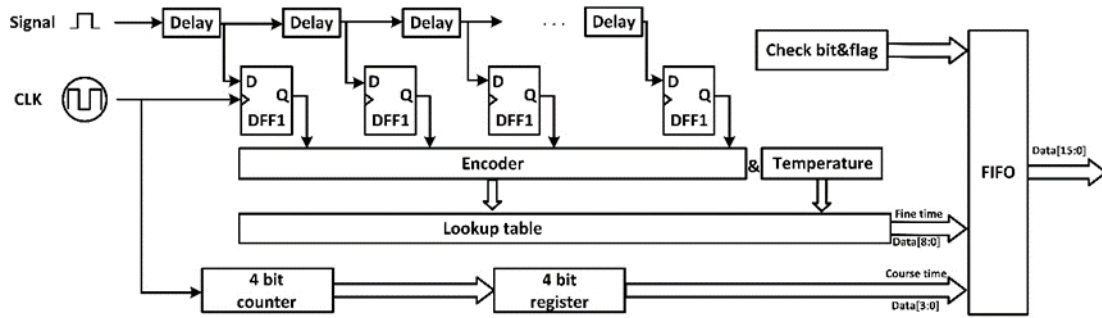

Fig3   Block diagram of the TDC

In the TDC structure, each delay chain is composed of 64 OR3 gates to interpolate the clock period, which has length of time exceeding the clock period, while only 16 CMOS buffers were employed in Ref. **4**. 64 DFFs are used to store the arrival time of start and stop signals in the form of temperature codes. Subsequently, the encoder converts the temperature code into a 6-bit binary code, representing uncorrected fine time. The 6-bit binary code and corresponding temperature utilizes the lookup table (LUT) to generate 9-bit fine time. The combination of coarse-time stored in 4-bit register and 9-bit fine time represents the time of an event signal. The time of flight was derived from Eq. (2)

$$\tau_{tof} = \left(N_{stop} - N_{start}\right) \times clk + \left(t_{start} - t_{stop}\right)$$

Where N_{stop} and N_{start} represents the 4-bit register's value of event signal. clk is the clock period, t_{start} and t_{stop} are 9-bit corrected fine time.

TMR technique have been adopted to mitigate SEU, because the prototype is planned to be placed on the Mars orbiter. But considering the power increase and speed decrease caused by TMR, it is only used in key registers [6].

2.2 Online Correction method

TDC based on time interpolation method implemented in FPGA has two problems. One is that the delay time of the delay unit is not uniform, the other is that the temperature change affects

the delay time of the delay unit. Both problems lead to performance degradation of TDC, owning to the large temperature variations environment on Mars, the mass spectrometer must work accurately within the temperature range of up to 100 °C. Consequently, it is essential to apply correction, which includes two kinds, correction and offline correction. Offline correction is to use the signal generator to test the code density, save the correction parameters of the delay units in the PC, which can be used to correct the results of flight time measurement. The disadvantage of offline correction is that it cannot get the corrected time measurement results in real time, so it is not conducive to the real-time operation of mass spectrometer. On the contrary, online correction stores correction parameters in FPGA, being convenient to correct results. As a consequence, online correction method based on LUT was adopted.

In the common methods, INL data are stored in LUT so that measured time can be corrected [7], which means actual time must be calculated in FPGA, leading to more logic resource usage. In contrast, in the adopted scheme, code density tests are performed [8], calculating the actual delay of each delay unit at a specific temperature, to make a LUT with temperature code as the address, so that it is not necessary for the prototype to calculate the actual delay in logic. Since the logic gates' delay time of FPGA can be affected by temperature, obviously, if the actual delay time for each temperature in the working range is stored in the LUT, the TDC will have the best accuracy. However, due to the temperature range, - 40 °C ~ + 60 °C, is relatively large, meanwhile, LUT is part of the FPGA's logic. The amount of logic resources of the FPGA only allows the delay time of partial temperature in the temperature range to be stored in the LUT. According to the test results in Ref. **7**, the performance of TDC has little change in a small temperature range. The whole temperature range is divided into several sections. In each section, the actual delay of the central temperature is stored in the lookup table. TDC in a temperature range is corrected by using the actual delay at the center temperature of the section.

3.   Test results

A large number of tests utlizing readout electronics were conducted, which aimed to evaluate its performance. Code density tests were used to get the code density and nonlinearity of the TDC, so that LUT can be calculated. Time measurement test was performed to obtain the corrected TDC's overall performance.
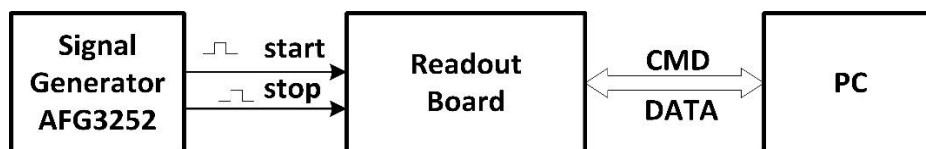
3.1 Calibration results

Fig.4 schematics of the TDC test

As shown in the Fig.4, code density tests were carried out. A large number of random signals with repetitive frequency that is different from TDC's reference clock, were input from the signal generator to the TDC, and the actual delay of the delay unit was obtained after data analysis and process. Test results showed the temperature changes within 5 °C had little effect on the performance of TDC. Therefore, the code density tests were carried out every 5 °C in the whole temperature range.
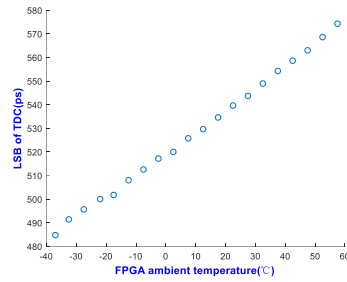
Fig.5 Drift of LSB from -40 ℃ to +60 ℃

Fig.5 shows the test results for one channel, apparently, the gate's delays vary almost linearly versus temperature. For a temperature range of -40 ℃ to +60 ℃, the LSB increases from 484.7 ps to 574.7 ps, which meet the requirement of the mass spectrometer. the LSB of the TDC increases by about 0.95 ps/ ℃. Based on the code density, the INL and DNL results of TDC were calculated.
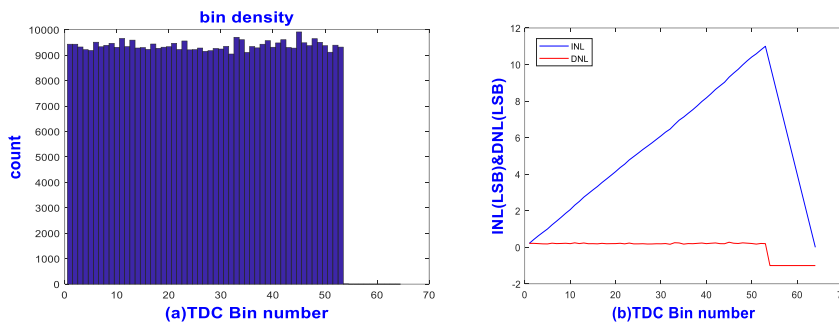

Fig.6(a)Statistical analysis of one channel TDC bins (22.5 ℃)

Fig.6 (b) the integral nonlinearity (INL) and differential nonlinearity (DNL) of one TDC channel in 22.5 ℃

Fig. 6(a) shows the hit counts of each TDC bin are different. The DNL and INL are shown in Fig.6 (b). The DNL and INL are mainly caused by the architecture of FPGA, the unequal bin widths in the delay chain contribute to most of the nonlinearity. The DNL is between -1/+0.2LSB, the INL is in the range 0/+11LSB. The integral nonlinearity is TDC's inherent error, therefore, the deviations caused by nonlinearity can be compensated.

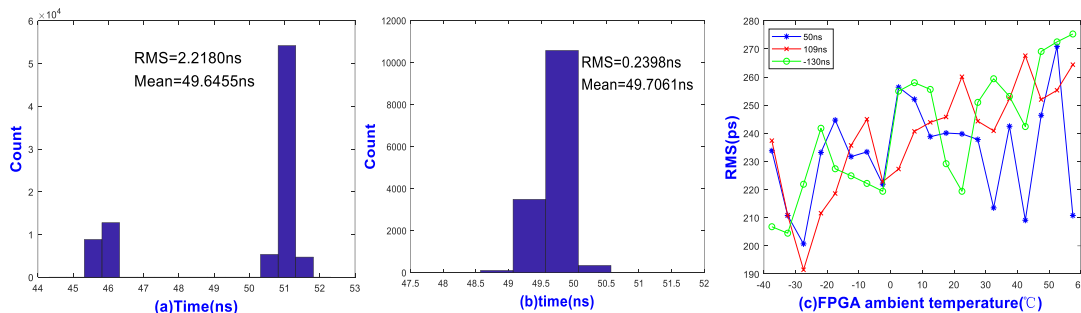## 3.2 Overall Performance of Time Measurement

Fig.8(a) uncorrected TDC test under: a 50 ns interval at 22 ℃(b) corrected TDC test under: a 50 ns interval at 22 ℃.
(c) TDC uncertainty test under: a 50ns interval at-40 ℃~+60 ℃

The test results are shown in Fig 8(a) and (b), without and with correction. Obviously, since the LUT compensate the nonlinearity and the LSB drift, TDC with correction got a higher precision. The online correction technology based on lookup table takes up a large amount of

logic resources, which may make the work of the FPGA unstable. For the reason of verifying the reliability of the system, a lot of tests have been performed. Like code density tests, two random pulses provided by AFG3252 generator with a repetitive frequency entered the TDC circuit as a pair of start and stop signals. A set of time measurements were performed with every 5 °C in the range of -40 ° C to +60 ° C. At each temperature, the fixed time interval increased from -170 ns in steps of 20 ns to +170 ns. Tests were performed for all channels and part of results are shown in Fig.8(c). It is obvious from the test results that the RMS of the TDC is always below 280 ps with time interval of 50 ns, 109 ns, -130 ns and FPGA's temperature of -40 °C to +60 °C. Moreover, extensive tests show the maximum time RMS is 305.5 ps when the time interval is between -170 ns and +170 ns.

4.   Conclusion

A design of readout electronics based on high-resolution time measurement has been successfully developed for Mars ion and neutral particle analyzer prototype, mainly comprised of TDC based on FPGA and data process FPGA. Overall test has been performed and shows that the TDC with online correction has a resolution of less than 600 ps with RMS of less than 310 ps in the range of -40 °C to 60 °C, which meets the requirement of mass spectrometer prototype applied in Mars mission.

Acknowledgments

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