PROCEEDINGS OF SCIENCE

DAQ platform based on SoC-FPGA for high resolution time stamping in cosmic ray detection

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Accurate timing in cosmic ray detection is critical for reconstruction of events from multiple scattered detectors. Since most of the detectors dedicated to study cosmic rays generate continuous analog signals, a precise timing depends on the sampling rate and the subsequent triggering system operating on the generated digital data stream. In this paper, a data acquisition platform based on a fully programmable System-On-Chip (SoC) and a high-speed analog to digital converter, able to manage 8-bit data resolution, 500MHz sampling rate and GPS connection for data synchronization is presented. The SoC is a ZYNQ 7000 device with a Field Programmable Gate Array (FPGA) and a dual core ARM processor embedded on a single chip.

The system achieves 2 ns time resolution and is also able to increase data amplitude resolution through oversampling and can simultaneously generate a real time histogram of the incoming data.

The platform has an embedded high voltage power supply control with temperature and pressure compensation for optimal and stable operation of different detectors.

While the time critical activities are handled and carried out by the FPGA, software running on the dual core ARM processor with a real time operating system (FreeRTOS) provides Ethernet connection for remote control of the platform.

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1. Introduction

High resolution timing is necessary to accurately correlate the data corresponding to specific cosmic rays events, as their duration may be in the scale of hundreds of nanoseconds, the time between events are in the same order of magnitude. In land observatories like in the Latin American Giant Observatory (LAGO) [1], each detector can be separated by long distances. To capture specific-energy events, and track the path of the cosmic rays (CR), many detectors must be triggered. As the absolute position of the detectors is known, a reliable way to reconstruct CR incoming direction is obtained by timing the delay between triggers on each detectors [2].

Fully-programmable SoC, FPGA-based devices, represent the state-of-art technology nowadays, which combines the versatility of high-level programming of a microprocessor and the concurrent and high-speed of a reconfigurable FPGA device in a single chip. This fusion of technologies enable the detectors to fully digest raw real-time data into processed information, allowing scientists to design higher precision instruments in smaller devices grabbing more data and reducing dead-time, thus increasing the measurement reliability of the experiments.

Finally, the increase of integration level with several types of sensors allows scientists to acquire secondary data, such as temperature, atmospheric pressure, light intensity, etc, allowing real-time data compensation and the effects under specific environmental conditions.

2. System Description

The main functions of the system are the following:

- High speed data acquisition from front-end.
- Preliminary data processing and storage.
- Read temperature and pressure sensors for baseline calibration.
- Read GPS signal and control the PPS (pulse per second) signal for time synchronization.
- Control the high voltage power supply and provide real time temperature and pressure compensation.
- Provide an Ethernet connection for remote data handling and control.

2.1 High speed data acquisition

To measure fast transient phenomena with high time-resolution, it has been selected the high performance and low power 8-bit 500 MSPS analog to digital Converter (ADC) ADC08500 [3]. This ADC de-multiplexes its digital data output to diminish the reading frequency by a factor of two. This board has been designed to fully exploit all main characteristics of the ADC including self-calibration, fine adjustment of input full-scale range and offset, and multiple ADC synchronization capability. This hardware module has three on board voltage regulators for reliable and low noise operation, and special protection circuits to avoid damages to the ADC due to out-of-range voltages or spikes in power supplies and input digital signals. The digital output data is

driven by 32 physical lines implementing 16 LVDS pairs at 250 MHz. These 45 digital signals are connected to a Low-Pin-Count FPGA mezzanine card (FMC) connector, and the PCB layout will be done according to the FMC standard ANSI/VITA 57.1-2008 This board, being a standard FMC module, can be managed with any commercial standard FMC Carrier like the one described in next section.

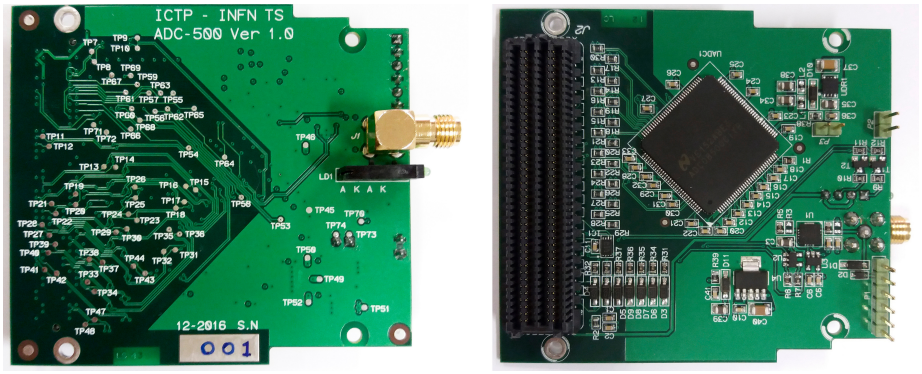


Figure 1: Top and bottom sides of the ICTP-INFN high-speed data acquisition FMC mezzanine board having one input analog channel 8-bits @ 500 MS/s.

2.2 FMC Carrier based on ZYNQ 7000, Zedboard

The system is built over a low-cost, commercial board Zedboard for the Xilinx-7000 All programmable SoC [4] for prototyping and debugging. It is build around a ZYNQ 7020 [5] device which combines a 'hard' dual core ARM processor with an FPGA fabric. The board provides several general purpose input and outputs for peripheral control and an Ethernet PHY for external communication. It also includes a high throughput low-pin count (LPC) FMC connector. The system developed for this application will be further explained on section 3.

2.3 Temperature and Pressure Sensors

Temperature and pressure values are obtained by ADT7420 and MS5611-01BA03 sensors. ADT7420 [6] is a high accuracy digital I2C temperature sensor. It also contains an internal band gap reference and a 16-bit ADC to monitor and digitize with 0.0078 C resolution. It is rated for operation over the -40 C to +150 C temperature range without any correction or calibration by the user. The MS5611 [7] is an integrated digital pressure sensor with SPI and I2C bus interface. The operating range is 10 to 1200 mbar and -40 to +85 C. The sensor module includes an ultra low power 24 bit ADC with internal factory calibrated coefficients, calculated and stored in the 128-bit PROM.

Both sensors are connected on the same bus using a dedicated I2C interface. Addressing, data reading, conversion and correction is done by the ARM processor on the ZYNQ without intervention of the FPGA part of the SoC.

2.4 High voltage Power Supply control

The system is designed to provide control to low-noise, miniature size high voltage DC/DC converter power supplies. It has been successfully tested on EMCO C20 [8] power supplies and ISEG BPS series [9]. Both power supplies are controlled by analog set voltage using a 16 bits precision digital to analog converter (DAC) MAX5216 using a SPI interface Peripheral Module. This DACs allows a stable, linear response on a loaded system in figure 2 is shown the correspondence curve of analog set voltage and high voltage output for a EMCO C20 HV power supply with an input buffer on the analog voltage set connected to a PMT on LAGO-Guatemala site. The output keeps a linear response until the buffer saturation point is reached.

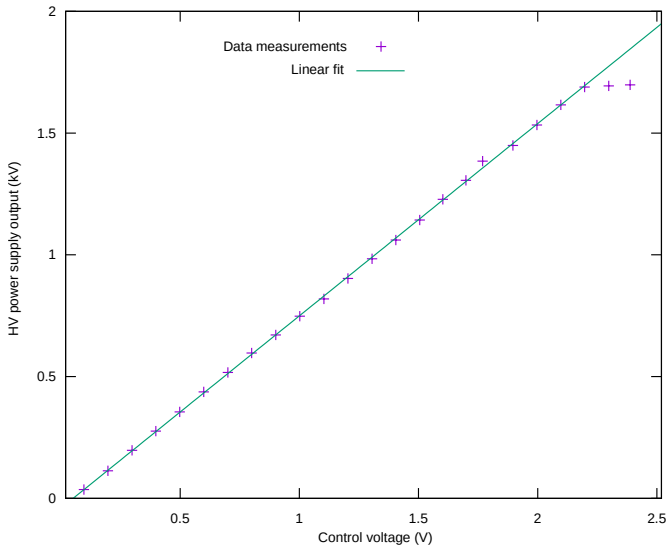


Figure 2: Output Voltage vs Programming Voltage DAC Input for EMCO C20 DC/DC Converter.

3. SoC hardware description

Figure 3 shows a block diagram describing the developed system on the ZYNQ device. It is divided in programmable logic design consisting on VHDL blocks developed on the FPGA part of the SoC, and processing system design consisting on software implemented on the ARM processor.

3.1 FPGA design

Time critical tasks are performed by the FPGA using custom made logic blocks. This tasks can be divided in: Timestamp and raw sample acquisition, signal analysis and diagnostic, peripheral controllers and FPGA-ARM communication.

The FPGA generates and provides to the ADC a 500 MHz clock signal. The ADC returns a raw data packet with a synchronization clock at half of the sampling frequency. Each packet consists on a 16 bits signal containing two 8 bits samples with the most recent sample found in the less significant byte.

The 250 MHz synchronization clock coming from the ADC is then synchronized with a PPS signal provided by the GPS. Both are used to generate a global clock inside a *Timestamp Generator*

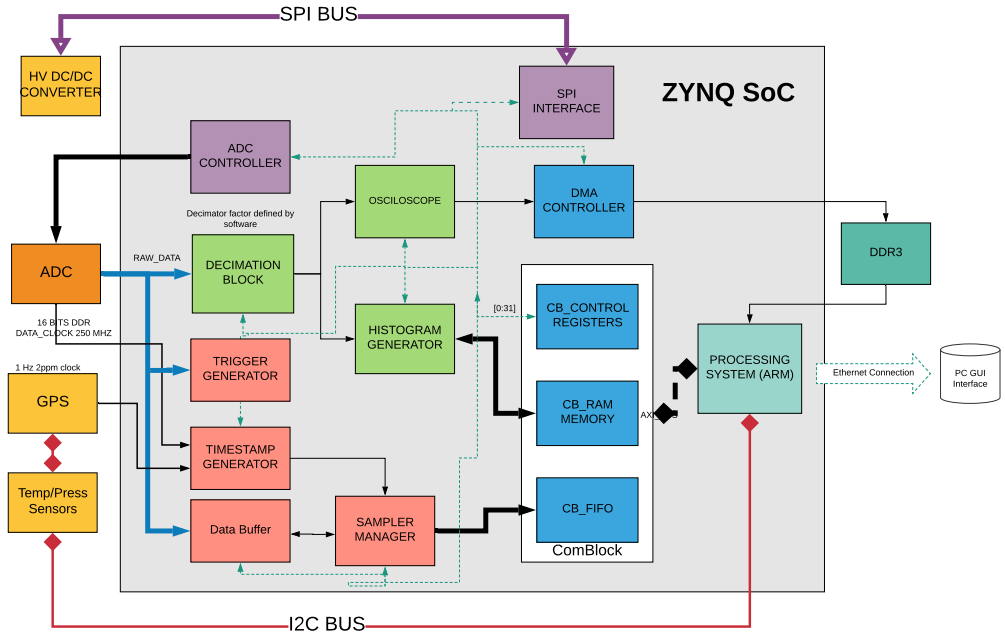


Figure 3: Functional diagram of the DAQ system implemented on the Zynq 7000 with peripherals. Timestamp and raw sample acquisition blocks are shown in red, signal analysis and diagnostic in light green, peripherals controllers in purple, FPGA-ARM communication in blue.

block. This block returns two 32 bit counters, a slow counter that keeps track of the PPS count in seconds, and a fast counter which counts the number of cycles of the synchronization clock from the ADC. The fast counter is cleared in each PPS rising edge as shown in figure 4.

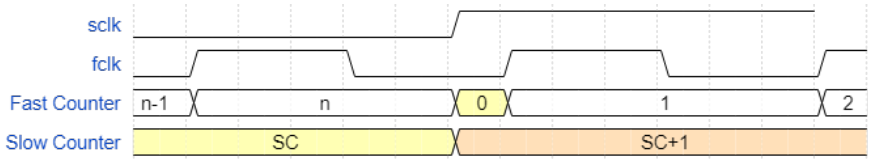


Figure 4: Time synchronization process

A *Trigger generator* block evaluates if the absolute value of the difference between consecutive samples is bigger than a threshold. This block also evaluates if the trigger condition happens between consecutive packages rising a *time correction* flag indicating that a timestamp needs to be corrected by one sampling period.

Raw data is stored on a RAM-based shift register with configurable delay. This *data buffer* allows to keep a variable number of samples before the trigger. When trigger condition is met, a *Sampler Manager* block creates a package with a configurable number of samples before and after trigger. This package is generated using a FIFO and the format of the package can be seen in figure 5.

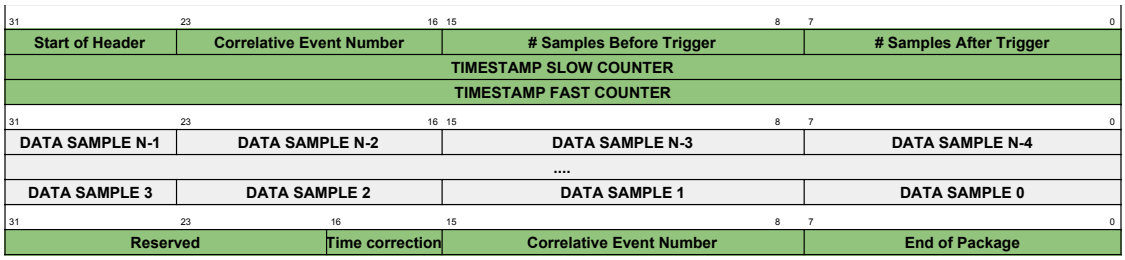


Figure 5: Package generated by *Sampler Manager* block stored on FIFO. .

The design also includes in-chip signal analysis and diagnostic blocks. Raw data is read by a decimation block which increases amplitude accuracy by oversampling. The implemented oversampling technique consists in accumulating N samples to increase the amplitude resolution in n_b in exchange of time resolution resulting in a decrease of the frequency in $f_{dec} = 500MHz/N$. The gain in number of bits can be seen in equation 3.1.

$$n_b = (8 + \frac{1}{2} Log_2 N) \tag{3.1}$$

An oscilloscope block allows to capture a trace of the decimated signal by providing standard tools such as trigger level selection, time position delay, rising, falling and auto trigger configuration. Captured trace is written by direct memory access (DMA) [10] into the DDR3-RAM memory for fast reading on the ARM processor.

A hardware generated histogram block is also provided. It works independently and in parallel with the oscilloscope block. The histogram is generated on a True Dual Port RAM memory (TDPRAM). Raw data input sets the address and the histogram block seeks the value stored on memory and makes an increment until the required number of samples is met.

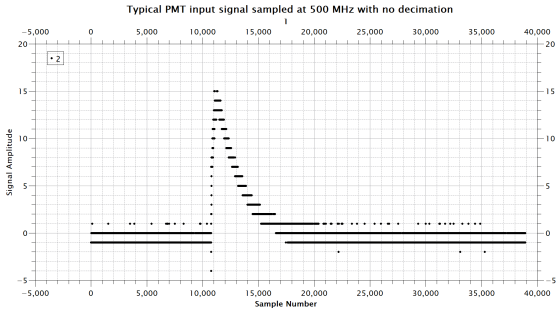
To interconnect the ARM microprocessor and the FPGA, a communication block (ComBlock) IP core [11] is used. This IP block is designed to simplify the interaction between the microprocessor and the FPGA by hiding the complexity of any specific bus by providing simple access to generic registers, TDPRAM memory and asynchronous FIFO. It communicates with the microprocessor using an AXI [12] Lite interface to control the registers and, to take advantage of burst operations, an AXI Full interface for the RAM and the FIFOs.

3.2 Processing system design

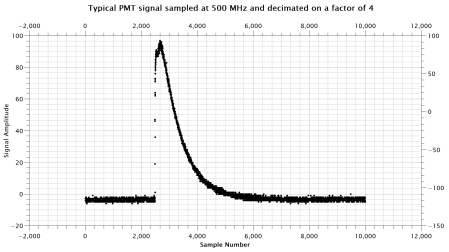
The microprocessor part of the SoC is in charge of complex activities such as perform specific math calculations, provide an Inter-Integrated Circuit (I2C) communication link with external hardware, provide a monitoring and management server for data exchange and control from a PC.

To interconnect the FPGA and the microprocessor we follow an approach of reconfigurable virtual instrumentation (RVI) as shown in [11]. The microprocessor runs a real time operating system to grant predictable timing and to provide data transmission through TCP/IP protocol. An application program interface (API) was designed to simplify the control over different hardware blocks that can be controlled via telnet.

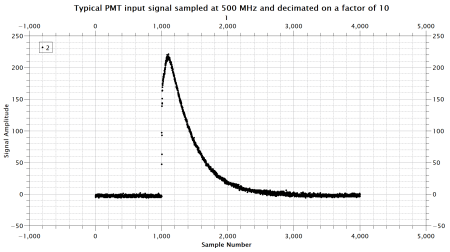
Some custom made functions were implemented to perform calibration calculations on some sensors, and baseline compensation based on temperature and pressure.



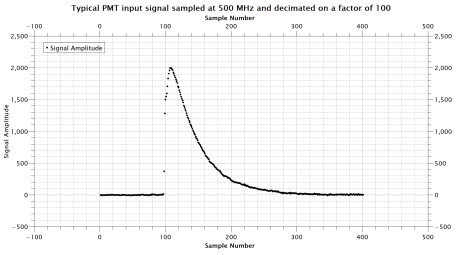
(a) No decimation, $T_s = 2ns$



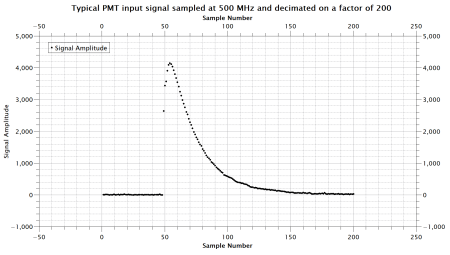
(b) Decimation Factor of 4, $T_s = 8ns$



(c) Decimation Factor of 10, $T_s = 20ns$



(d) Decimation Factor of 100, $T_s = 200ns$



(e) Decimation Factor of 200, $T_s = 400ns$

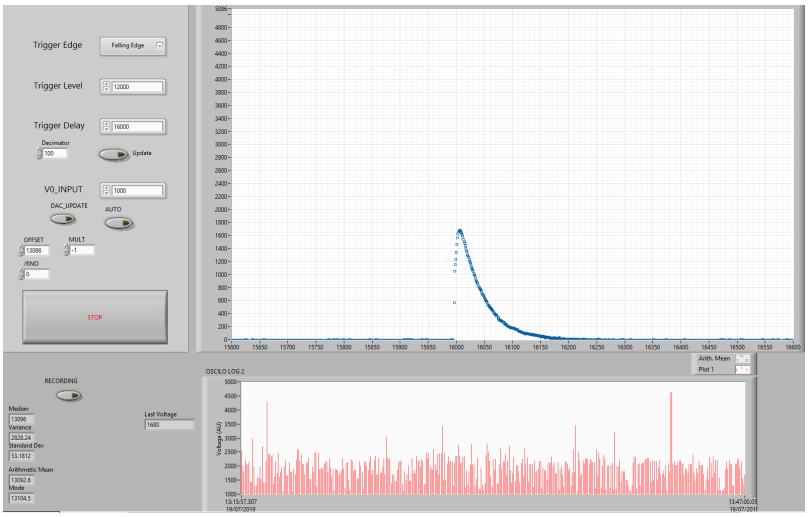
Figure 6: Typical PMT trace, captured at different decimation factors over the same window of time (80 μs.)

4. Data acquisition and Graphical User Interface (GUI)

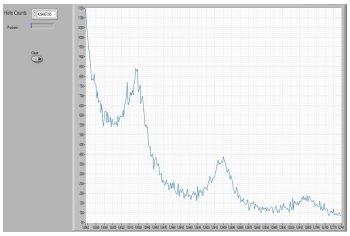
Figure 6 shows different data traces captured in a 80 μs window, using our system connected to a PMT EMI 9821Q base [13]. The sampled window is set to capture 20 μs before the trigger condition and 60 μs after. In sub-figure 6a is shown the maximum sample rate that the system is able to acquire, the period between samples (T_s) is set at 2ns and the maximum data resolution achievable is 8 bits. At 2ns is easier to set a timestamp, but for slower inputs, like the one presented, quantization error are visible along the trace.

Using the decimation blocks, signal resolution is increased at cost of number of samples as shown in figures 6b, 6c, 6d, 6e. This can be set independently of the timestamp sus-system and can be configured sending parameters to the management server or by using a GUI (as shown in figure

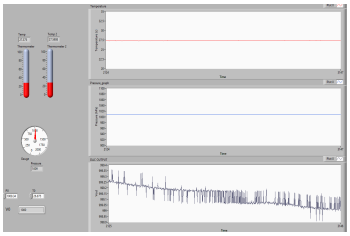
7).



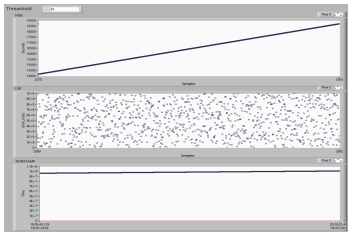
(a) Main window, and Oscilloscope



(b) Histogram Generator



(c) Temperature and pressure control and compensation



(d) Timestamp status and control

Figure 7: Graphical User Interface build in Labview 2018

5. Conclusion

The design of a generic DAQ plattform based on SoC-FPGA gives flexibility for addressing several applications common in cosmic ray detectors. The RVI approach simplifies migration of the FPGA design between SoC devices allowing to reuse the hardware in platforms other than Zedboard. This DAQ has been tested on CIAA_ACC board [14] with few modifications on the hardware and the software. The high speed data rate from the ADC together with the signal analysis and diagnostic blocks allows to condition the system to the signal regarding their speed.

In the context of Water Cherenkov Detectors (WCD) experiments where particles create Cherenkov emissions within a water volume, PMT tubes collect the light producing an analog signal which then is sampled using high speed ADCs [15]. Experiments like Pierre Auger [16], and LAGO, need autonomous stations able to link to remote acquisition centers. Tools like the histogram generator, oscilloscope and decimation blocks can be used for self calibration routines. The monitoring and management server simplifies the interconnection and data transmission on a network and the GPS allows to locate the position of each detector and provides a reliable time base for synchronization between multiple stations.

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