PROCEEDINGS OF SCIENCE

The Phase-II upgrade of the ATLAS muon spectrometer

Antonio Policicchio*, **on behalf of the ATLAS Collaboration**
Sapienza Università di Roma and INFN Roma1, Italy
E-mail: antonio.policicchio@roma1.infn.it

The muon spectrometer of the ATLAS detector will undergo a major upgrade foreseen for the Phase-II, in order to cope with the operational conditions at the high-luminosity LHC. The trigger and readout electronics for the Resistive Plate Chambers (RPC), Thin Gap Chambers (TGC), and Monitored Drift Tube (MDT) chambers will be replaced to make them compatible with a new trigger scheme with higher trigger rates and longer latencies. MDT precision chambers will be integrated into the hardware trigger in order to sharpen the momentum threshold. The MDT front-end electronics will also be replaced. New-generation RPC chambers will be installed in the inner barrel layer to increase the acceptance and robustness of the trigger. Some of the MDT chambers in the inner barrel layer will be replaced with new small-diameter MDTs. New TGC triplet chambers in the barrel-endcap transition region will replace the current TGC doublets to suppress the high trigger rate from random coincidences in this region. A major upgrade of the power system is also planned. The Phase-II upgrade concludes the process of adapting the muon spectrometer to the ever increasing performance of the LHC, which started with the New Small Wheel Phase-I upgrade project that will replace the innermost endcap wheels.

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*Speaker.

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1. Introduction

The High-Luminosity upgrade of the LHC (HL-LHC) will provide pp collisions at a center-of-mass energy of $\sqrt{s}$ = 14 TeV with luminosities up to 7 $\times$ 10^{34} cm^{-2} s^{-1} and a total integrated luminosity of 3000 fb^{-1}. The ATLAS detector [1] will undergo a major upgrade in order to cope with these new conditions and to fully exploit the HL-LHC physics potential. The upgrade of ATLAS follows two steps: the Phase-I upgrade during Long Shut-down 2 (LS2, 2019–2020), followed by Run 3, and the Phase-II upgrade during LS3 (2024–2026), followed by HL-LHC runs. The challenge for the muon spectrometer (MS) is to preserve its muon identification and tracking performance in much harsher conditions in terms of particle rates, radiation, and number of inelastic pp interactions per bunch crossing. The trigger must become more selective, so that the low p_T thresholds required for many physics studies and searches result in an acceptable trigger rate, and acceptance should possibly overcome the present limitations in geometrical acceptance.

2. The Muon Spectrometer

The ATLAS muon spectrometer [2] consists of three large air-core superconducting toroidal magnets (two endcaps and one barrel) providing a field of approximately 0.5 T on average. The deflection of the muon trajectories in the bending plane of the magnetic field is measured via hits in three layers of monitored drift tube (MDT) precision chambers covering the region in pseudorapidity $|\eta| < 2.7$. In the innermost endcap wheels of the MS, cathode strip chambers (CSC) are used instead of MDTs in the region $2.0 < |\eta| < 2.7$. Three layers of resistive plate chambers (RPC) in the barrel ($|\eta| < 1.05$) and 3-4 layers of thin gap chambers (TGC) in the endcaps ($1.05 < |\eta| < 2.4$) provide the muon trigger, and also measure the muon trajectory in the non-bending coordinate of the magnets. In the CSC, MDT, and RPC systems the MS is sub-divided in azimuthal direction (ϕ) into 16 sectors, eight large (L) and eight small (S). In the TGC system, there are instead 24 or 48 equal-sized sectors in ϕ, depending on the radial position. The inner, middle, and outer layers of the barrel and endcap chambers are labeled BI, BM, BO and EI, EM, EO, respectively. In the barrel-endcap transition region ($1.05 < |\eta| < 1.3$), muons are detected in the EIL4, EE (extra), and EM layers. The endcap disks made of the CSC and EI1–3 chambers are also referred to as the Small Wheels (SW), the EM1–5 disks as the Big Wheels (BW). The locations of the current detectors in the MS for small and large sectors are shown in Figure 1 (black text).

The hardware trigger level is based on hit coincidences between different RPC or TGC detector layers inside programmed geometrical windows which define the muon p_T. The maximum rate and latency of this first-level trigger are 100 kHz and 2.5 μs, respectively. The high-level trigger level performs a full track reconstruction and a refined p_T measurement by using also precision chamber hits.

In the Phase-I upgrade [3], foreseen for LS2, the SW will be replaced by the New Small Wheels (NSW) using small-strip TGC (sTGC) and Micro-Mesh Gaseous Structure chambers (MM) used for both triggering and precision tracking. In the barrel-endcap transition region ($1.05 < |\eta| < 1.3$), the MDT chambers will be replaced by integrated stations of new generation RPC and small-diameter MDT (sMDT) chambers to enhance the trigger coverage (the BIS78 project). The locations of the new Phase-I upgrade detectors are shown in Figure 1 (green text).

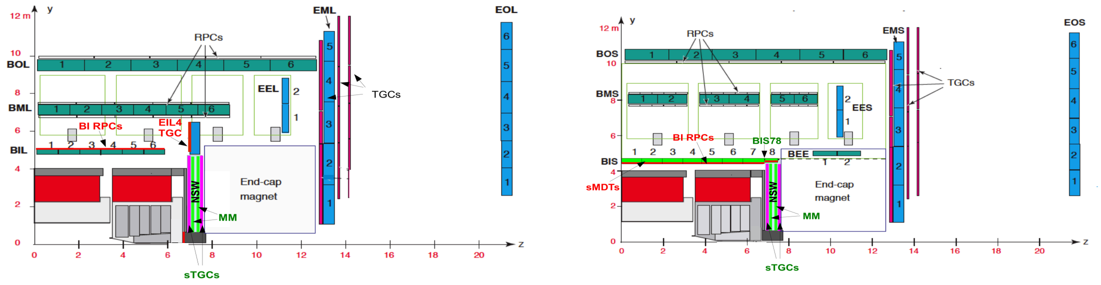

Figure 1: $R-Z$ view of the MS layout in a large (left) and in a small sector (right), showing the new detectors to be installed for Phase-I (green text) and Phase-II upgrades (red text), and those that will remain unchanged from the present layout (black text) [4].

3. Muon spectrometer Phase-II upgrade

Considering that the small wheel will be replaced by the NSW during Phase-I upgrade, the reconstruction efficiency and momentum resolution of the MDT system will be robust against high pile-up and high background rates and the muon identification and reconstruction performance will not be degraded by the higher particle rates and backgrounds of the HL-LHC. The muon trigger requires instead significant upgrades to maintain the same trigger momentum thresholds while keeping the trigger rates at a manageable level. The lowest-level muon trigger should be able to trigger on single muons with high efficiency, with a rate of less than 40 kHz for a threshold of $p_{\mathrm{T}} > 20$ GeV. The sharpness of the turn-on curve of the trigger, and the reduction of fake triggers from low-momentum muons which dominates the total muon trigger rate, is limited by the spatial resolution of the RPC and TGC trigger chambers. The efficiency of the trigger is high in the endcap regions, but is limited in the barrel region by the geometrical acceptance of the RPC system, which is below 80% for tracks detected in three RPC chambers. The Phase-II hardware trigger (L0 trigger) will be based on muon and calorimeter information and will have a latency of 10 μs so that more complex trigger algorithms than in the present system will be feasible, and it will send events to the high trigger level at a rate of 1 MHz. The Phase-II upgrade of the MS [4] comprises the installation of new chambers, the replacement of some existing chambers, and the replacement of a large part of the front-end and trigger and readout electronics. Indeed the electronics currently mounted in the ATLAS Muon Spectrometer cannot be used for a L0 trigger able to handle a 1 MHz frequency. Programmable external FPGAs will be used to make coincidences, instead of the present custom ASICs on detectors, making the new trigger more robust, simple and flexible. The readout electronics on detectors will be replaced by data multiplexers and high bandwidth optical links to send out hit information from the detectors to the L0 trigger logic. The high and low voltage power system will also be replaced, to ensure operation through the full HL-LHC data taking. Figure 1 (red text) shows the locations of the Phase-II detectors in the large and small sectors of the MS.

3.1 RPC chambers and electronics

To maintain a high trigger efficiency, new RPCs will be installed on the inner MDT chambers of the barrel. The present RPCs, to ensure their continued operation at the HL-LHC, will have to be operated at reduced voltage to respect the original design limits on currents and integrated charge. Hit inefficiencies up to 35% are estimated. This would reduce the trigger efficiency in the barrel region to an unacceptable level. Despite the lowered single-hit efficiencies, a high trigger efficiency and purity can be maintained by loosening the requirements on hit coincidences in the current chambers, if at the same time a coincidence is requested with new RPCs introduced in the inner barrel as shown in Figure 2 (left). The installation of these chambers will also cover most of the acceptance holes of the present barrel muon trigger. In total 276 new triplet RPCs will be built. Similar chambers are currently being built for the BIS78 project. The new RPCs will have a thinner gas gap than the current RPCs (1 mm instead of 2 mm), and operate at 5400 V instead of 9600 V. The effective threshold for front-end electronics is expected to be 0.1 mV compared to 1 mV used for the present RPCs. A new high-sensitivity frontend ASIC integrating discriminator, time-to-digital converter (TDC), and serializer are being developed using the SiGe BiCMOS technology. A Data Collector and Transmitter board is under development and it will be mounted on the detectors and will collect data from front-end electronics and send it to the off-detector via optical fibers.

3.2 sMDT chambers and sMDT/MDT electronics

In small sectors, the new RPC chambers can only be installed if the present MDT chambers are replaced by new sMDT chambers with reduced overall thickness so that the sMDT chambers and the new RPCs fit in the same envelope as the original MDT chambers. In the large sectors, there is sufficient space available to add the new RPCs without replacing the MDTs. The tubes of the sMDT chambers have half the diameter of the original MDT (15 mm instead of 30 mm), and operate at 2730 V instead of 3080 V, resulting in the same field strength around the wire. In total 96 sMDT chambers will be built for the Phase-II upgrade. 14 similar chambers have been built for other regions of the ATLAS detector and were operational during LHC Run 2. In addition, 16 similar chambers are being built for the BIS78 project. The trigger and readout chains for both MDT and sMDT chambers will be upgraded and the information of the precision chambers will be available at the L0 trigger level. The triggerless MDT readout and the Phase-II trigger rate and latency require the production of about 18000 front-end cards (known as mezzanine boards) for the replacement of the ones mounted on MDT chambers and the equipment of the new sMDT chambers. The mezzanine boards will include custom amplifier-shaper-discriminator (ASD) and TDC ASICs. Good progress has been made for the design and test of the new electronics, and the pre-production of the ASD ASIC has already started. About 1200 Chamber Service Modules will collect the time measurements from mezzanines and will send them off-detector to a MDT Data Processor board, where relevant hits are extracted out of the raw data stream. The use of the precision MDT chamber information at the L0 trigger level will result in an improved trigger muon momentum resolution and thus in a sharper p_{T} threshold. The single-muon trigger rates for a p_{T} threshold of 20 GeV will be decreased from 45 - 85 kHz to 15 kHz in the barrel region and from 15 - 20 kHz to 10 kHz in the endcap region.

3.3 TGC chambers and electronics

To obtain a uniform level of purity for triggered muons, the current TGC doublet chambers at $1.05 < |\eta| < 1.3$ will be replaced by TGC triplets, the EIL4 TGCs. The trigger rate in the endcaps is dominated by fake muon triggers from low-p_{T} charged particles generated inside the endcap toroid cryostats. Requiring a coincidence of the BW TGCs with chambers in front of the cryostats greatly reduces the rate of these fake triggers, and this is one of the motivations for the NSW and BIS78 projects. The EIL4 TGCs cover the region around the NSW, at $1.05 < |\eta| < 1.3$ in large sectors (small sectors will be covered by the BIS78 RPCs). The present doublet chambers have a coarse readout granularity, which in high-background conditions results in a large rate of random coincidences with background hits. With the new triplet chambers a more robust coincidence logic can be used, requiring hits in two out of three planes, and smaller coincidence windows will reduce the rate of random coincidences to a negligible level. The TGC electronics will be upgraded to transfer the data to the off-detector electronics. A prototype has been already produced few years ago, it has been tested during the 2018 run to check the communication and the effects of single-event upset. New prototypes will be build at the beginning of 2020 and a full slice test is foreseen by the end of the year. Figure 2 (right) shows the expected efficiency for the L0 endcap muon trigger relative to offline muons for a p_{T} threshold of 20 GeV with a single muon Monte Carlo simulation sample for the HL-LHC scheme, and data taken in 2018 for the Run-2 scheme. The HL-LHC scheme provides a higher efficiency in the plateau region and a better p_{T} resolution in the turn-on curve.

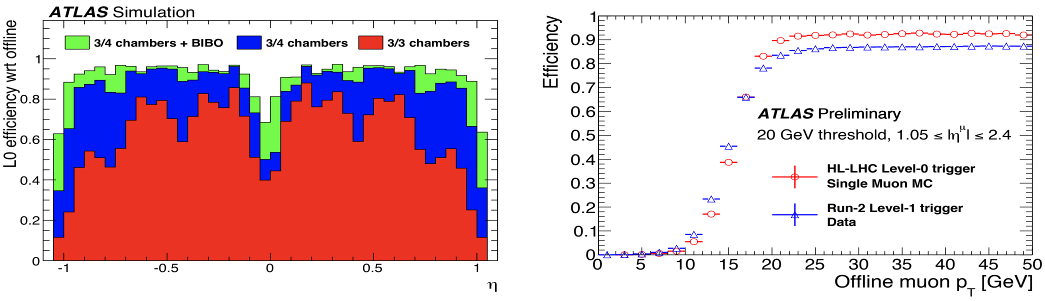

Figure 2: Left: efficiency times acceptance of the L0 barrel trigger with respect to reconstructed muons with $p_{\mathrm{T}} = 25$ GeV as a function of η, assuming the worst-case scenario: the histogram shows the efficiency of the existing 3/3 chambers trigger, of the 3/4 chambers trigger including the inner layer, and the additional gain from the additional 2/4 chambers BI-BO trigger [4]. Right: Expected efficiency for the L0 endcap muon trigger relative to offline muons for a transverse momentum threshold of 20 GeV with a single muon Monte Carlo simulation sample for the HL-LHC scheme, and data taken in 2018 for the Run-2 scheme [5].

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