PROCEEDINGS OF SCIENCE

New Level-1 jet feature extraction modules for ATLAS phase-I upgrade

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After the Long Shutdown 2 (Dec. 2018 – Feb. 2021), the LHC will be a new machine in many respects and produce collisions with a center-of-mass energy at or near 14 TeV. The instantaneous luminosities can be expected to reach 2×10^{34} cm^{-2}s^{-1}, which is two times the original design value. The mean number of interactions per bunch crossing is expected to go up to 80. To meet the challenges of the high-luminosity environment (much higher event rates and pileup level), several major upgrades will be installed during the Long Shutdown 2 in the ATLAS detector. As a part of the updates, the Level-1 calorimeter trigger will be upgraded to exploit higher granularity data compared to those available during Run 2 by using a new system of feature extraction modules, which each reconstructs different physics objects at Level-1.

The Jet Feature Extractor (jFEX) is one of three feature extraction modules and has been conceived to identify small-/large-area jets, large-area τ leptons, missing transverse energy and the total sum of the transverse energy. The Xilinx Virtex UltraScale+ FPGA fulfills the physics requirements of significant processing power and large input bandwidth within a tight latency budget. The modular design optimizes a large number of high-speed signals within the limited space of an ATCA board. To guarantee the signal integrity, the board design has been accompanied by simulation of the power, current, and thermal distributions. The printed circuit board has a 24-layer stack-up and uses the MEGTRON6 material, which is commonly used for signal transmission above 10 Gb/s.

This contribution focuses on the technological aspects of the jFEX module, reporting on the simulation studies and the design solutions of the board. Two jFEX prototypes and one pre-production module have been produced and tested at CERN with other systems, and these test results are presented. The firmware implemented on the trigger board will be illustrated in connection with the FPGA performance and board power consumption. The whole jFEX system, consisting of 6 boards, will be produced by the end of 2019 to allow the installation and commissioning of the full system in time for the LHC restart at the beginning of 2021.

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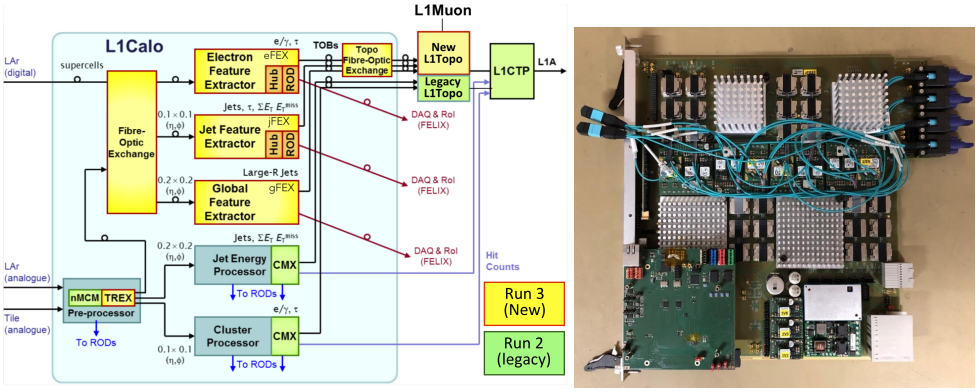
1. Introduction

After the Long Shutdown 2 (LS2, Dec. 2018 – Feb. 2021), the LHC will undergo several upgrades and produce collisions with a center-of-mass energy at or near 14 TeV. The instantaneous luminosities are expected to reach 2×10^{34} cm^{-2}s^{-1}, which is two times the original design value. To meet the challenges of the high-luminosity environment (much higher event rates and pileup level), several major upgrades will be installed during the LS2 in the ATLAS detector [1]. As a part of the updates, the Level-1 calorimeter (L1Calo) trigger will be upgraded to exploit finer granularity data than Run 2 by using a new system of 3 feature extraction (FEXs) modules: electromagnetic FEX (eFEX) [2], jet FEX (jFEX) [3] and global FEX (gFEX) [4]. Figure 1(a) shows the L1Calo system for the Phase-I upgrade [5]. The components in yellow highlight the newly introduced system after LS2. The legacy system will be dismissed once the new system is fully commissioned.



(a) (b)

Figure 1: (a) The L1Calo System in LHC Phase-I [5], The newly introduced modules are highlighted in yellow. The legacy system (in green) will be dismissed once the new system is fully commissioned. (b) The jFEX pre-production module fully equipped with four Xilinx Virtex UltraScale+ FPGAs.

The jFEX sub-system receives data from the electromagnetic and hadronic calorimeters, and identifies jets and large-area τ particles. Global variables like total transverse energy ($\sum E_{\mathrm{T}}$) and missing transverse energy ($E_{\mathrm{T}}^{\mathrm{miss}}$) are also calculated. These calculations are performed by algorithms in parallel. The jFEX will send Trigger Objects (TOBs) to the Level-1 Topological processor (L1Topo), that will forward the information to the L1 Central Trigger Processor (L1CTP), where the final L1 trigger decision will be made. The jFEX fulfills the link speed specification of the input optical links, which is 11.2 Gb/s. The output optical link speeds to L1Topo has been set to 12.8 Gb/s. The data rate for readout is 6.4 Gb/s. As a part of the Phase-I upgrade, the jFEX will be installed in the ATLAS electronics cavern USA15 and operated during Run 3. In Phase-II (from 2024), jFEX will be operated as a part of Level-0 Calorimeter Trigger System [6].

2. jFEX module

The jFEX subsystem consists of six modules covering a η range from -4.9 to 4.9 for both LAr and Tile calorimeters. Four modules cover the *central region* ($|\eta| < 2.4$), and two modules cover the *forward region* ($2.4 < |\eta| < 4.9$). Figure 1 (b) shows the jFEX pre-production module.

Each jFEX module consists of an Advanced Telecommunications Computing Architecture (ATCA) mainboard (double width) and mezzanine cards. The modular design optimizes a large number of high-speed signals within the limited space of an ATCA board. It holds a significant processing power and a large input bandwidth (up to 3Tb/s). In order to find TOBs in a single core area, Physical Medium Attached (PMA) loopback for on-board data duplication is enabled to assure enough environment areas for trigger towers in the boundary. The mainboard carries the real-time processing circuitry: 4 processor FPGAs (XCVU9P-2FLGA2577E), connected with 24 MiniPOD devices (20 receivers and 4 transmitters). Four exact copies of the FPGA/MiniPOD circuitry are placed on the same Printed Circuit Board. Module control via IPBus is implemented on the control mezzanine. An IPBus interface provides high-level functional control of jFEX modules. It is a protocol that runs over Ethernet and provides register-level access to the hardware. The FPGA configuration memories are also located on the control mezzanine, along with the timing, trigger and control (TTC) reception and conditioning. The control mezzanine runs along the lower part of the front panel; it allows for easy front panel connectivities and controls. Environmental monitoring and low-level control are implemented on an Intelligent Platform Management Controller (IPMC) module. The primary power supply is realized via standard PIM/converter bricks. The secondary power supplies are located on mezzanines.

3. Hardware Characterization

Figure 2 shows the fiber routing for jFEX testing with LAr Trigger Processing Mezzanine (LATOME) in Surface Test Facility (STF) at CERN. One L1Topo and one Feature-extractor Test Module (FTM) are also connected as an extra input source. The 48 fiber outputs from the jFEX transmitters are also looped into receivers. In total, there are 48 optical links from LATOME, 96 optical links from FTM, 48 optical links from L1Topo, and 48 fiber outputs from jFEX transmitters looped in receivers. In addition, the data duplication via PMA loopback is enabled in this test. The TTC clock was received from the FTM via backplane using a TTC-VMEbus Interface (TTCvi) and a transmitter module (TTCvx) with a 40.08 MHz oscillator. The Integrated Bit Error Ratio Test (IBERT) uses PRBS31 at 11.2 Gb/s input rate for more than 24 hours and error-free, the bit error rate is less than 1×10^{-15} per line. The eye diagrams with the largest open area for 4 different optical inputs from 4 processor FPGAs are shown in Figure 3 (a). Figure 3 (b) shows the eye diagrams with the largest open area for 4 different PMA loopback links from 4 processor FPGAs.

The Xilinx Virtex UltraScale+ specifications for the Multi-Gigabit Transceiver (MGT) reference clock are defined in the frequency domain. It is important to measure the jitter of the clock. The measurement has been performed in collaboration with the CERN Electronic Systems for Experiments group. A signal generator provides a 40.08 MHz clock directly to the jitter cleaner, which sits on the mezzanine. The clock is distributed on the mainboard using multiple fanouts. The probed clock signal is gathered through MMCX (micro-miniature coaxial) connectors on the board. The measurements with comparing to the Xilinx specifications are shown in Table 1. The clock signal is within the Xilinx specifications.

The MGTs on the Virtex UltraScale+ are very sensitive to noise on its power rails, which needs to be below a maximum of 10 mVpp noise on the FPGA power pins over the band from 10 kHz to 80 MHz. The measurement was performed using MMCX connectors soldered on the pad of the

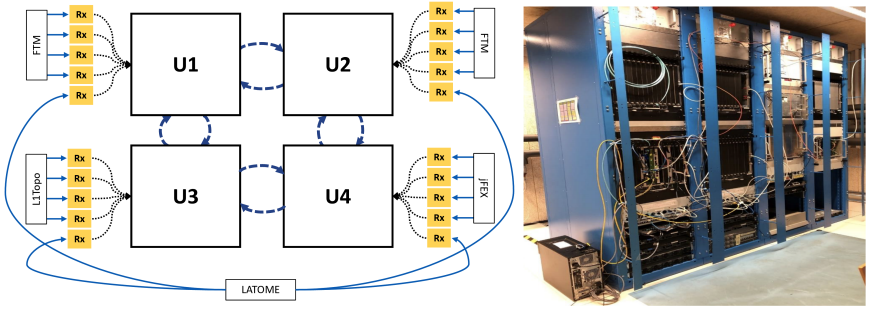
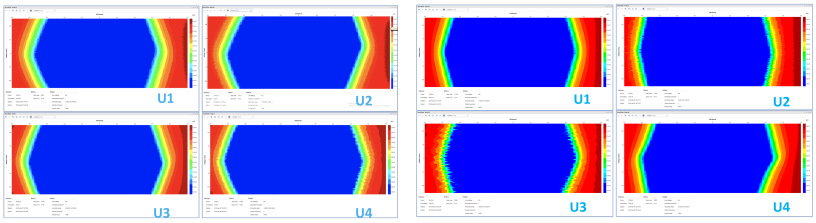


Figure 2: The setup of fiber routing at STF using one LATOME, one L1Topo, and two FTMs as input source. The 48 fiber outputs from the jFEX transmitters are also looped into receivers. The data duplication via PMA loopback is enabled. The dashed lines show the electrical connections, and the solid lines stand for the optical connections.



(a) (b)

Figure 3: Eye diagrams with the largest open area for 4 different (a) optical inputs and (b) PMA loopback links from 4 separate processor FPGAs.

Offset Frequency	Xilinx Specifications	jFEX Measurement
10 kHz	−112 dBc/Hz	−137.14 dBc/Hz
100 kHZ	−128 dBc/Hz	−143.83 dBc/Hz
1 MHZ	−145 dBc/Hz	−147.615 dBc/Hz

Table 1: Jitter measurement results for three frequencies compared with Xilinx specifications.

decoupling capacitor of the voltage rails. The scope was AC coupled, set at high impedance with external 50 Ω termination and the scope bandwidth was limited to 80 MHz according to the Xilinx specifications. Table 2 shows the ripple measurement of V_{MGTAVTT} and V_{MGTAVCC}. The values are less than 10mV for all the processors which are within the Xilinx specifications.

FPGA	$V_{\text{MGTAVCC0.9V}}$ (mV)	$V_{\text{MGTAVTT01.2V}}$ (mV)
U1	1.63	1.51
U2	2.99	2.90
U3	4.02	3.17
U4	4.07	2.79

Table 2: Ripple measurement of V_{MGTAVTT} and V_{MGTAVCC} (peak to peak) for all the four processor FPGAs.

An optical link attenuation test is performed using a loop-back on the jFEX pre-production module and a variable attenuator. Two high-speed links are tested on jFEX by adding optical at-

tenuation on the fiber chain. In the case of data rate at 11.2 Gb/s, errors show up when attenuation arrives at 12.25 dB. For the case of data rate at 12.8 Gb/s, errors show up when 7.25 dB of attenuation is given.

Figure 4 shows the power consumption of all four processor FPGAs in jFEX pre-production module with all MGTs activated and with the IBERT firmware. The estimates of the FPGA power consumptions and voltages from Vivado Design Suite are also reported. Measured current consumption is consistent with Vivado estimates, and the FPGA internal temperatures are within the Xilinx specifications.

Supply	Voltage Rail	Voltage	Current (A)	Temp. (°C)	Efficiency*	Output Power (W)	Input Power* (W)
Board Level Voltages	1V8	1.80	0.80	25.97	70.0%	1.44	2.05
	2V5	2.50	12.79	32.00	93.0%	31.97	34.38
	3V3	3.30	7.12	27.00	93.0%	23.50	25.26
U1	$V_{CCINT\ (0.85V)}$	0.85	14.26	36.00	92.0%	12.12	13.18
	$MGTYAV_{CC\ (0.9V)}$	0.90	6.97	40.00	85.0%	6.27	7.38
	$MGTYAV_{TT\ (1.2V)}$	1.20	18.57	43.00	87.0%	22.28	25.61
U2	$V_{CCINT\ (0.85V)}$	0.85	13.97	29.70	92.0%	11.87	12.91
	$MGTYAV_{CC\ (0.9V)}$	0.90	7.22	34.00	85.0%	6.50	7.64
	$MGTYAV_{TT\ (1.2V)}$	1.20	18.36	36.00	87.0%	22.03	25.32
U3	$V_{CCINT\ (0.85V)}$	0.85	14.53	41.00	92.0%	12.35	13.42
	$MGTYAV_{CC\ (0.9V)}$	0.90	7.51	43.00	85.0%	6.76	7.95
	$MGTYAV_{TT\ (1.2V)}$	1.20	18.56	48.00	87.0%	22.27	25.60
U4	$V_{CCINT\ (0.85V)}$	0.85	14.44	39.00	92.0%	12.27	13.34
	$MGTYAV_{CC\ (0.9V)}$	0.90	7.32	40.00	85.0%	6.59	7.75
	$MGTYAV_{TT\ (1.2V)}$	1.20	18.49	47.00	87.0%	22.19	25.50
Total (W)						220.42	247.31

*estimation based on datasheet

Current Estimation@12V (A)	18.37	20.61

Current Estimation Vivado (A)	
$V_{CCINT\ (0.85V)}$	14.91
$MGTYAV_{CC\ (0.9V)}$	11.524
$MGTYAV_{TT\ (1.2V)}$	24.406

SLOT 5 XADC	
FPGA	Temp. (°C)
U1	45.00
U2	40.00
U3	41.00
U4	43.00

SLOT 11 XADC	
FPGA	Temp. (°C)
U1	57.00
U2	44.00
U3	48.00
U4	47.00

Figure 4: Details of power consumption of the four processor FPGAs for jFEX pre-production module.

4. Conclusions

The jFEX subsystem from the ATLAS experiment at the LHC will identify small/large-R jets, large τ, $\sum E_{\mathrm{T}}$, and $E_{\mathrm{T}}^{\mathrm{miss}}$ at Level-1 using high-granularity calorimeter data with significant processing power and huge input bandwidth (up to 3Tb/s). The design has been completed, built and demonstrated to work successfully. The full production of final jFEX modules will be completed by the end of 2019, followed by installation and commissioning in 2020.

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