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ATLAS Trigger and Data Acquisition Upgrades for the High Luminosity LHC

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On behalf of the ATLAS collaboration.

The ATLAS experiment at CERN has started the construction of upgrades for the "High Luminosity LHC", with collisions due to start in 2026. In order to deliver an order of magnitude more data than previous LHC runs, $\sqrt{s}$ =14 TeV protons will collide with an instantaneous luminosity of up to 7.5×10^{34} cm^{-2}s^{-1}, resulting in much higher pileup and data rates than the current experiment was designed to handle. While this is essential to realize the physics program, it presents a huge challenge for the detector, trigger, data acquisition and computing. The detector upgrades themselves also present new requirements and opportunities for the trigger and data acquisition system. The approved baseline design of the TDAQ upgrade comprises: a hardware-based low-latency real-time Trigger operating at 40 MHz, Data Acquisition which combines custom readout with commodity hardware and networking to deal with 5.2 TB/s input, and an Event Filter running at 1 MHz which combines offline-like algorithms on a large commodity compute service augmented by hardware tracking. Commodity servers and networks are used as far as possible, with custom ATCA boards, high speed links and powerful FPGAs deployed in the low-latency parts of the system. Offline-style clustering and jet-finding in FPGAs, and track reconstruction with Associative Memory ASICs and FPGAs are designed to combat pileup in the Trigger and Event Filter respectively. This paper will report recent progress on the design, technology and construction of the system. The physics motivation and expected performance will be shown for key physics processes.

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1. Introduction

The High Luminosity Large Hadron Collider (HL-LHC) project [1] is planned to begin operation in the second half of 2026. Protons at $\sqrt{s}$ =14 TeV will collide with an instantaneous luminosity of up to 7.5×10^{34} cm^{-2}s^{-1}. As a consequence, higher pileup and data rates than the current experiment was designed to handle are expected. Despite these adverse conditions, it is important to keep the p_{T} of the various trigger objects, as shown in Figure 1, as low as possible.

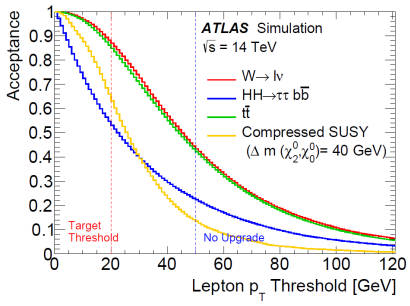


Figure 1: Integrated acceptance as a function of the single lepton p_{T} threshold for four representative channels [3].

The HL-LHC running conditions represent a huge challenge for the ATLAS detector, trigger, data acquisition and computing. For this reason, an upgrade, termed the "Phase II" upgrade, of both the machine and the experiment will occur in the Long Shutdown 3 between 2024-2026.

2. ATLAS TDAQ Phase-II Upgrade

The Phase-II upgrade of the ATLAS TDAQ [2, 3] system will satisfy the broad ATLAS physics programme planned for the HL-LHC, while coping with ultimate HL-LHC conditions.

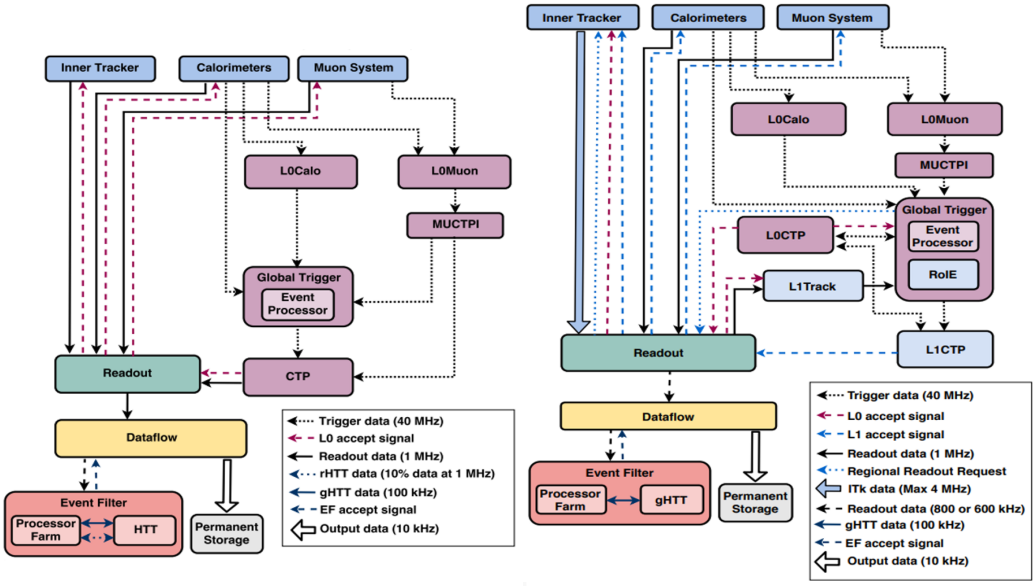
TDAQ is composed of three main systems: the Level-0 Trigger System, the Data Acquisition (DAQ) System and the Event Filter System. A baseline architecture, based on a single-level hardware trigger with a maximum rate of 1 MHz and 10 μs latency, is presented in Figure 2(a).

The baseline architecture will be capable of evolving to a dual-level hardware trigger architecture, shown in Figure 2(b), where the systems in light blue are the additional components. The two main metrics for the evolution are the hadronic trigger rates and the inner pixel detector layer occupancy. If either is higher than expected, the baseline TDAQ architecture would restrict the trigger menu. The baseline architecture is described in these proceedings.

2.1 L0 Trigger

The Level-0 Trigger system is made up of the Level-0 Calorimeter Trigger (L0 Calo), Level-0 Muon Trigger System (L0 Muon), Global Trigger and Central Trigger subsystems.

L0 Calo The L0 Calo sub-system is based on the Phase-I electron Feature EXtractor (eFEX), jet Feature EXtractor (jFEX), and global Feature EXtractor (gFEX) complemented by a new forward EXtractor (fFEX). It uses calorimeter (Liquid Argon and Tile) data with coarse granularity to identify and calculate:

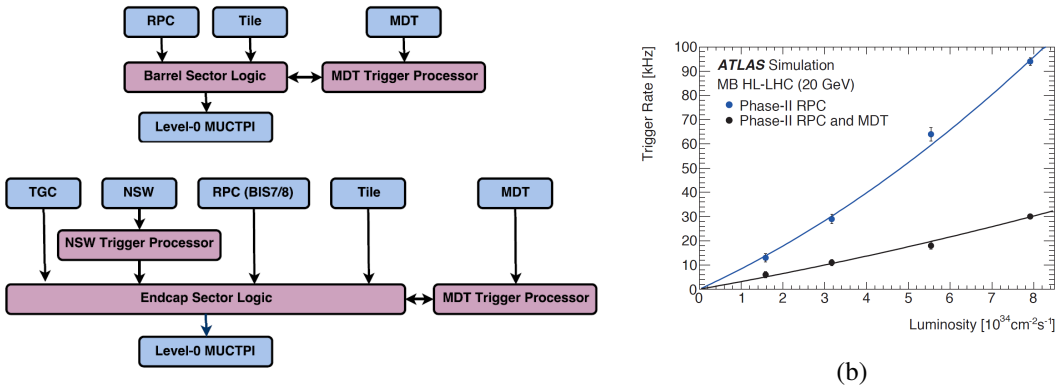


(a) (b)

Figure 2: Comparative diagrams between the TDAQ System in Phase-II baseline 2(a) and evolved 2(b) scenarios [3].

- eFEX: electron and photon object,
- jFEX: single jets,
- gFEX: large R (or multi jet) triggers and global quantities, and
- fFEX: forward electromagnetic (forward jet) trigger objects at high η.

L0 Muon The L0 Muon system receives data from the upgraded Muon spectrometer and the Tile calorimeter. Trigger performance improvements include both acceptance and momentum resolution. The New Small Wheel (NSW) Trigger Processor will be used to determine not only the deflection angle with Thin Gap Chambers (TGC) in the Sector Logic but also the deflection angle and the sagitta in the Monitored Drift Tube (MDT) Trigger Processor for a refined momentum



(a) (b)

Figure 3: In 3(a) simplified block diagram of the barrel (top) and endcap (bottom) L0 Muon Trigger System. In 3(b) rate estimation of the L0 single-muon trigger without and with MDT for the barrel region [3].

resolution. Additional Resistive Plate Chambers (RPCs) will be installed in the innermost barrel layer. Moreover, L0 Muon will take advantage of the MDT information. In fact, the selectivity of the current Level-1 muon trigger is limited by the moderate spatial resolution of the RPC and of the TGC. During the Phase-II Upgrade, MDT chambers will be included, as shown in Figure 3(a), in L0 Muon and will provide better spatial resolution and p_T resolution close to that of the offline reconstruction. The contribution of the new MDT chambers can be seen in Figure 3(b), showing how the rate of L0 single-muon trigger, based on RPC plus MDT in the barrel region, is lower than the rate with RPC only.

Global Trigger The new Global Trigger system uses full-granularity calorimeter information to run offline-like algorithms. It refines the trigger objects from L0 Calo and L0 Muon by applying topological selections (such as angular requirements). An example of the performance of the combined L0 Calo and Global Trigger is shown in Figure 4(a).

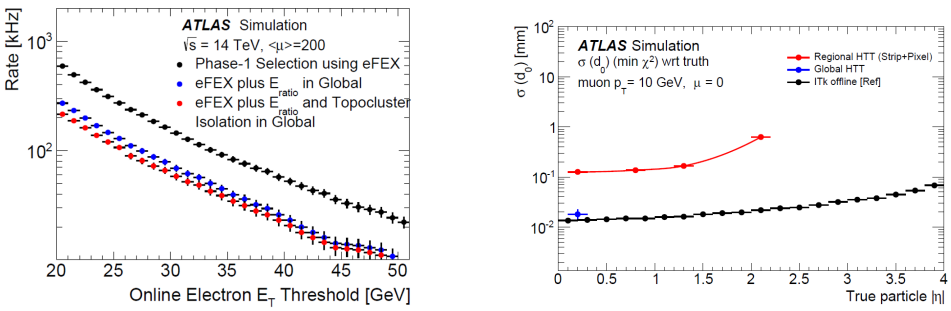
Central Trigger subsystems The Muon Central Trigger Processor Interface (MUCTPI) aggregates and merges the trigger information from barrel and endcap muon systems, then sends it to the Global Trigger and the Central Trigger Processor(CTP). The CTP makes the final L0 Accept decision after aligning and combining all the digital trigger inputs, introducing preventive deadtime and applying prescales as required.

2.2 Data Acquisition

The Data Acquisition (DAQ) system is composed of two sub-systems, as shown in Figure 2, the Readout system (in green) and the Dataflow system (in yellow).

The Readout system receives data from the ATLAS detector front-end electronics at the L0 trigger rate (1 MHz), performs basic processing and sends data to the Dataflow system. The two main components are the FrontEnd LInk eXchange (FELIX), a server-based system that uses a custom PCIe card to interface with the detector electronics, and the Data Handlers, which are servers performing detector-specific formatting and monitoring tasks.

The Dataflow system buffers data before, during and after the Event Filter decision, providing partial and full event access as needed, and transfers data to permanent storage.



(a) (b)

Figure 4: In 4(a) level-0 rate as a function of leading p_T for the single-electron/photon triggers. In 4(b) comparison of d_0 resolution in the Hardware Track Trigger and in offline reconstruction. [3].

2.3 Event Filter

The Event Filter (EF) system provides high-level trigger functionality. It consists of a CPU-based processing farm complemented by Hardware-based Tracking for the Trigger (HTT) co-processors. The high pile-up conditions give rise to higher occupancy of tracking detectors and reduced energy resolution in calorimeters. This negatively affects e.g. the separation of electrons from background jets, the calculation of global event quantities like $E_{\mathrm{T}}^{\mathrm{miss}}$ and jet energy resolution. To maintain a menu with thresholds similar to Run 1 and Run 2, the EF has to use algorithms close to the offline reconstruction methods, as well as tracking to identify a primary vertex and associate reconstructed objects with it.

Processor Farm The current baseline assumption is that commodity servers will provide the required compute density on the time-scale of Phase-II, with an estimated farm size of 4.5 MHS06[1], to handle a L0 rate of 1 MHz together with HTT. At the same time, commodity processors and accelerators (GPGPU and FPGA) to make use of optimized reconstruction software, specialized fast algorithms or machine learning techniques are under investigation for EF tracking.

Hardware Track Trigger HTT is a new massively parallel system, based on FPGA and custom Associative Memories (AM ASICs). It receives ITk data and provides fast hardware-based track reconstruction. Some of the advantages of this technology are low power consumption and short latency. Moreover, the HTT will take advantage of the FTK [6] experience and enable a simple transition into the dual-level hardware trigger system.

The HTT includes regional (rHTT) and full-scan (gHTT) track reconstruction capabilities. In regional tracking, partial tracker event data (from the 8 outermost layers) are sent from the Event Filter Processing Unit (EFPU) to HTT for track reconstruction ($p_{\mathrm{T}} > 2$ GeV). EFPU uses then rHTT tracks in combination with Global Trigger objects to reduce the rate to 400 kHz. If required, full-ITk data tracking is performed by HTT for tracks with $p_{\mathrm{T}} > 1$ GeV. EFPU uses gHTT tracks, in combination with offline-like analysis, to the reduce the rate to 10 kHz. In Figure 4(b) the comparison of d_0 resolution for rHTT and gHTT fitting and offline is shown.

In the Evolved Scenario, rHTT has moved to the Level-1 hardware-based trigger. The associated event rejection then takes then place before the EF.

3. Trigger Menu

Figure 5 shows a schematic flow from the representative set of physics goals to the L0 Trigger items needed to achieve them. The middle column lists the corresponding triggers required. For example, the Global Trigger enables a low-p_{T} electron trigger at Level-0, and then regional tracking reduces the high rate early in the Event Filter processing. Definite plans for the Run 4 trigger menu will come towards the end of Run 3.

[1] More info about HEP-SPEC06 (HS06) unit can be found at this link: http://w3.hepix.org/benchmarking.html

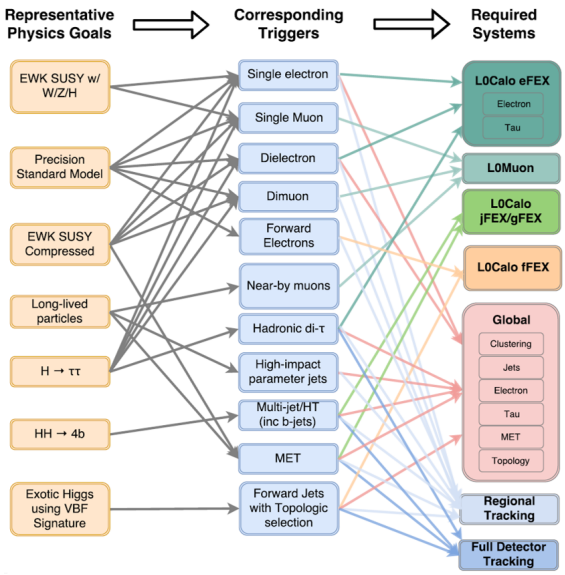


Figure 5: Schematic summary of the flow from the representative set of physics goals to the L0 Trigger items [3].

4. Conclusion

Plans for the ATLAS TDAQ systems for the HL upgrades are detailed in a Technical Design Report [3]. The TDAQ system enables a broad physics program for the HL-LHC with a baseline scenario. It also accommodates a possible evolution, eventually driven by high hadronic trigger rates and high occupancy in the inner pixel detector layer.

The L0 Trigger and the DAQ systems rely on the knowledge gained during LHC Run 1 and 2, as well as on Phase I experience. Some components need to be upgraded while some new ones are going to be added to sustain the increased event size and trigger rates.

The HTT tracking information is used to reduce event rates, offering good flexibility and modularity to run at both regional and global level, and the capability to evolve to a dual-level hardware trigger system, as part of L1 trigger.

References

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