PROCEEDINGS OF SCIENCE

The Phase-II Upgrade of the ATLAS Muon Spectrometer

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ATLAS will upgrade its muon spectrometer for high-luminosity LHC runs. The number of trigger layers will increase in both barrel (by adding a new layer of Resistive Plate Chamber - RPC) and endcap (by upgrading the EIL4 Thin Gap Chambers - TGC) regions. To create space for the additional layer of RPCs in small sectors, the present Monitored Drift Tube (MDT) chambers need to be replaced by small-diameter MDT chambers. A TGC tracking trigger will be implemented using segments found by TGC chambers in the endcap middle station and by the New Small Wheel (NSW) detector in the endcap inner station. MDT data will be used for the first time at the first trigger level to improve the trigger muon momentum resolution. In addition, most electronics will be replaced to handle higher data rates and longer latency expected at high-luminosity LHC runs. All muon spectrometer upgrade activities are on track for an installation starting at the beginning of 2024.

XXIX International Symposium on Lepton Photon Interactions at High Energies - LeptonPhoton2019
August 5-10, 2019
Toronto, Canada

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PoS(LeptonPhoton2019)070

1. Introduction

The ATLAS muon spectrometer at the Large Hadron Collider (LHC) is the world's largest muon spectrometer [1]. It is composed of three stations (inner, middle and outer) in both barrel and endcap regions with toroid magnets providing a field of approximately 0.5 T. It can perform standalone muon momentum measurement with a resolution of about 10% for 1 TeV muons. Monitored Drift Tubes (MDT) are used as precision-tracking chambers and cover the pseuorapidity range of $|\eta| < 2.7$, except the endcap inner station (EI) where Cathode Strip Chambers (CSC) are used in the region $2 < |\eta| < 2.7$ due to their higher rate capability and time resolution. Resistive Plate Chambers (RPC) and Thin Gap Chambers (TGC) are used as fast trigger chambers in the barrel ($|\eta| < 1.05$) and endcap ($1.05 < |\eta| < 2.4$) regions, respectively.

For the ongoing Phase-I upgrade, the EI station will be replaced by a new small wheel (NSW) detector composed of eight layers of Micromegas and eight layers of small-strip TGC [2]. In addition, for the barrel inner (BI) station, each small-sector MDT chamber in stations #7 and #8 (BIS78) will be replaced by a small-diameter MDT (sMDT) chamber and a thin-gap RPC.

The overall Phase-II upgrade strategies [3, 4] are: (1) increase the number of RPC and TGC trigger layers in the barrel and endcap regions, respectively; (2) combine TGC and NSW information to reduce fake trigger muons found in the endcap region; and (3) use MDT as a trigger device at the first trigger level to improve the trigger muon momentum resolution. For the BI station, an extra layer of thin-gap (1 mm) RPC triplets will be added to make the barrel trigger more robust. For BI small sectors, the present MDT chambers need to be replaced with sMDT chambers to create space for the addition of a new RPC layer. For the EI station, the current EIL4 TGC chambers will be upgraded from doublet to triplet. Most electronics will be upgraded to cope with the Phase-II trigger and latency requirements. A TGC tracking trigger will be implemented using segments found by both TGC and NSW, and MDT data will be used at the first trigger level. Figure 1 shows the layout of the upgraded muon spectrometer for small and large sectors.

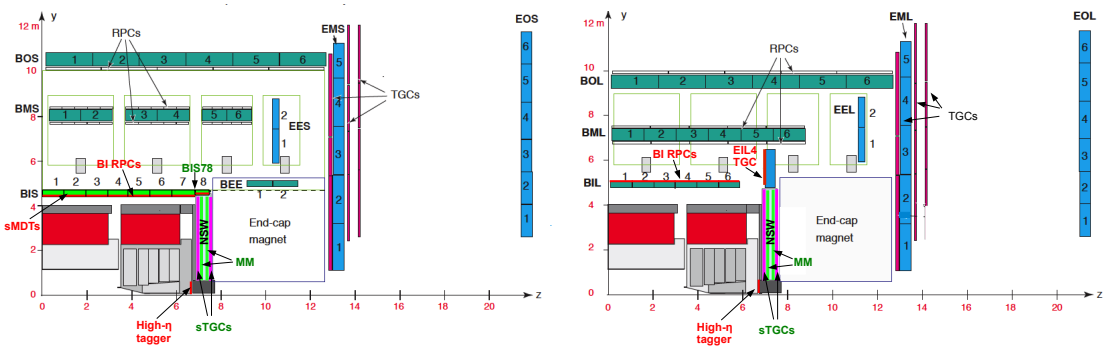

Figure 1: Two $r-z$ views of the Phase-II ATLAS muon spectrometer layout showing a small sector (left) and a large sector (right). The drawings show the new detectors to be added in the Phase-II upgrade (red text: BI RPC, sMDT, EIL4 TGC, high-η tagger). A high-η tagger is under consideration to extend muon identification in the region $2.7 < |\eta| < 4.0$, but it is not discussed in this proceeding.

For high-luminosity LHC runs, it is expected that we will have a lower operating high voltage

for the RPC detector in order to reduce the aging effects. For the worst-case scenario, the resulting single-hit efficiency will be 65–85% depending on η. Figure 2 (left) shows the efficiency of the 3-out-of-3 (3/3) chambers trigger corresponding to the high-p_{T} trigger used in Run 2, the 3/4 chambers trigger including the BI layer, and the additional gain from the 2/4 chambers BI-BO trigger. The overall RPC trigger efficiency increases from $\sim 65\%$ to $\sim 90\%$. Figure 2 (right) shows trigger turn-on curves for three different assumptions of muon momentum resolution at the first trigger level. With the sMDT used at the first trigger level, the single-muon trigger rates for a p_{T} threshold of 20 GeV will be decreased from $45-85$ kHz to 15 kHz in the barrel region and from $15-20$ kHz to 10 kHz in the endcap region.

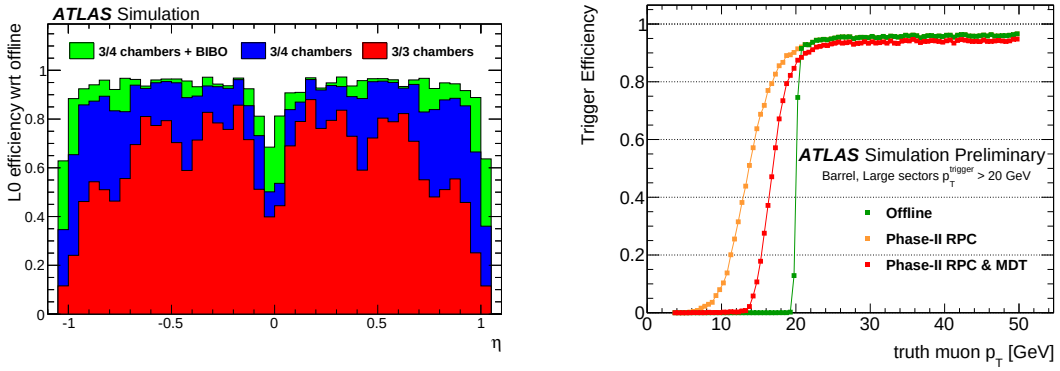

Figure 2: Left: Efficiency times acceptance of the barrel trigger for muons with $p_{\mathrm{T}} = 25$ GeV as a function of η. Right: Trigger efficiency as a function of the true muon p_{T} for three different cases: with offline momentum resolution, using Phase-II RPC, and using Phase-II RPC and MDT.

2. sMDT chambers and MDT/sMDT electronics

In total 96 sMDT chambers will be built for the Phase-II upgrade. Each sMDT chamber has about 500 tubes with a diameter of 15 mm and a length of 1.5 m [5]. The chamber R&D was completed a few years ago, and 14 similar chambers have been built for other regions of the ATLAS detector and were operational during LHC Run 2. In addition, 16 similar chambers are being built for the BIS78 upgrade. The BIS1-6 chamber layout and envelopes have been defined and drift tube design has completed. The chamber design is expected to be finished in 2019. Figure 3 (left) shows a prototype sMDT chamber built at MPI Munich. Current MDT electronics were mounted to study the chamber performance.

Figure 3 (right) shows the upgraded trigger and readout chains for both MDT and sMDT chambers. The MDT on-chamber electronics will send all muon hits to the circuitry in the ATLAS counting room. Signals from MDT tubes are processed by an amplifier-shaper-discriminator (ASD) [6] chip and subsequently time-digitized by a time-to-digital converter (TDC) [7] chip. These time measurements are transmitted through a Chamber Service Module (CSM) to a MDT Data Processor board, where relevant hits are extracted out of the raw data stream. For this hit extraction, timing information from the fast trigger chambers (RPCs in the barrel and TGCs in the endcap) is used as the reference time to find the hit drift time in the tube and the drift time is converted into the distance of the track from the wire. These precision coordinates of all matched hits

are then processed. Segment finder and track fitter algorithms are applied to determine the muon momentum. Time information for hits matching the first-level trigger time window (L1 accept) is stored for transmission to the FELIX readout system after receiving the first-level trigger accept signal. Good progress has been made for the designs of ASD, TDC, CSM and MDT data processor board. The ASD design was finalized in 2018 and 10% of the chips needed have been produced. The v1 TDC chips have been produced and tested, the v2 design containing all needed features will be submitted in fall 2019. The v2 CSM prototype will be designed and tested by the end of 2019, and the MDT data processor board is currently under design.

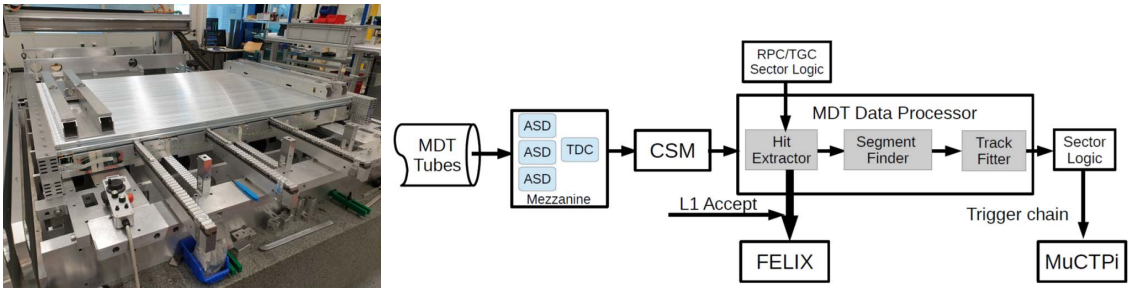

Figure 3: Left: A BIS1-6 sMDT prototype chamber built at MPI Munich. Right: Block diagram of the trigger and readout electronics for both sMDT and MDT chambers.

3. RPC chambers and electronics

In total 276 new triplet RPCs will be built for the Phase-II upgrade [8]. Similar chambers are currently being built for the BIS78 upgrade and a singlet RPC chamber is shown in Figure 4 (left). The BIS1-6 chamber envelopes have been defined and optimizations with the chamber layout, such as supporting structure, number of chamber types to be built, and installation strategy, are ongoing. In addition, there are ongoing studies for the design of the RPC singlet. We are looking for a lighter dielectric filler material used for readout strip panels. We also plan to readout strips from both ends to obtain η and ϕ coordinates simultaneously.

More sensitive electronics are required to read out detector signals from thin-gap RPCs. For example, the effective threshold for front-end electronics is expected to be 0.1 mV compared to 1 mV used for the present RPC chambers in the barrel region. A new frontend ASIC integrating discriminator, TDC, and serializer will be designed using the SiGe process. A one-channel prototype integrating the discriminator and TDC is currently under test. A Data Collector and Transmitter board that receives the RPC data and sends the muon hits to the sector logic is under development.

4. EIL4 chambers and TGC electronics

EIL4 TGCs are located in the EI region covering $1.0 < |\eta| < 1.3$. They were not originally designed to be part of the trigger system, and therefore are not optimized for this use. Current EIL4 chambers are made of doublets with a single unit with an area of ~ 1 m^2. These chambers will be replaced by triplets with finer granularity and coordinates for all three layers will be read out to complete the trigger coverage in the EI station.

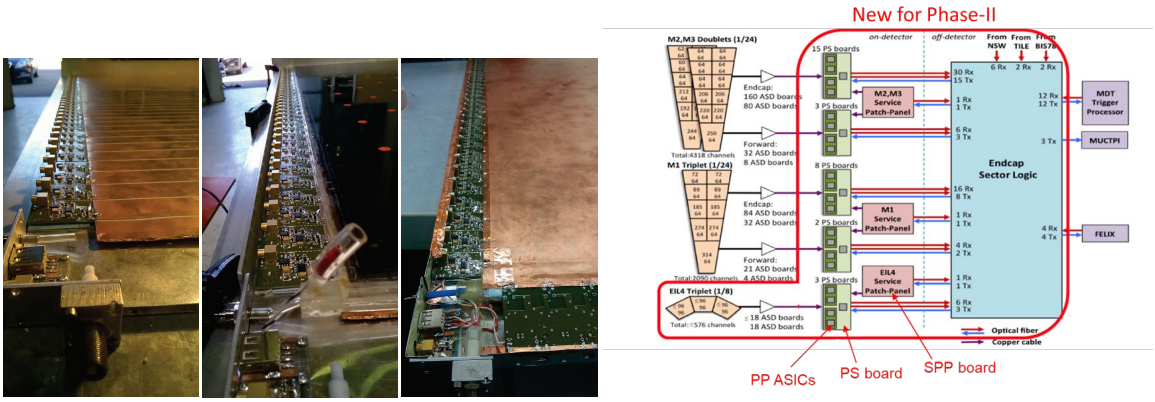

Figure 4: Left: BIS78 singlet RPC prototype. The ϕ strip panel (left) is covered by the gas gap (centre) with the gas inlet shown in the foreground. The sandwich is finished up by the η panel (right). Right: Schematic diagram of the TGC electronics.

Figure 4 (right) shows the block diagram of the upgraded TGC electronics [9]. The PS boards receive the signals from ASD boards, perform time alignment with a PP ASIC, and transfer the data to the off-detector electronics. The Endcap Sector Logic (SL) boards receive the signals from PS boards. Each SL board has one FPGA for data readout and trigger processing. The design for the new PP ASICs has been finished and all chips were produced. A PS prototype board was installed in ATLAS during Run 2 to study SEU effects on Kintex-7 FPGA and all SEUs were automatically recovered. The TID qualification tests of board components were performed using a Co^{60} source. Conceptual design and hardware demonstration are expected to be finished in 2019.

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