PROCEEDINGS OF SCIENCE

The ATLAS Hardware Track Trigger design towards first prototypes

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In the High-Luminosity LHC, planned to start with Run 4 in 2026, the ATLAS experiment will be equipped with the Hardware Track Trigger (HTT), a dedicated hardware system able to reconstruct tracks in the silicon detectors with short latency. This HTT will be composed of about 700 ATCA boards, based on new technologies available on the market, like high-speed links and powerful FPGAs, as well as custom-designed Associative Memory ASIC (AM), which are an evolution of those used extensively in previous experiments and in the ATLAS Fast Tracker (FTK). The HTT is designed to cope with the expected extreme high luminosity in the so called "L0 only" scenario, where HTT will operate at the L0 rate (1 MHz). It will provide good quality tracks to the software-based High-Level-Trigger (HLT), operating as coprocessor. It will allow for a reduction of the HLT farm size by a factor of 10, by lightening the load of the software tracking. All ATLAS upgrade projects are also designed for an evolved, so-called "L0/L1" architecture, where part of HTT is used in a low-latency mode (L1Track), providing tracks in regions of ATLAS at a rate of up to 4 MHz, with a latency of a few micro-seconds. This second phase poses very stringent requirements on the latency budget and to the dataflow rates. All the requirements and the specifications of this system have been assessed. The design of all the components has been reviewed and validated with preliminary simulation studies. After these validations are completed, the development of the first prototypes will start. In this paper we describe the status of the design review, highlighting the technical challenges and required specifications, towards the preparation of the first slice tests with real prototypes.

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1. The Hardware Track Trigger project

The High-Luminosity LHC (HL-LHC) project, planned to start with Run 4 in 2026, will increase the LHC instantaneous luminosity by a factor between five and seven. This will lead to an increase in the number of collisions per bunch crossing (pileup) from around 40 in Run 2 to around 200. In this challenging environment, trigger rejection can be increased by using tracks reconstructed in the Inner Tracker (ITk). However, CPU timing increases very rapidly with pileup, implying an unfeasible increase in the necessary computing resources. Hardware tracking is an option to perform fast tracking reconstruction at the trigger level. At HL-LHC the ATLAS experiment will be equipped with the Hardware Track Trigger (HTT) system, a dedicated hardware system able to reconstruct tracks with short latency.

The HTT will be based on FPGAs and custom-designed Associative Memory (AM) ASICs, which are an evolution of those used in the ATLAS Fast Tracker (FTK) [1]. Two different architectures are foreseen: a baseline (L0 only) scenario and an evolved (L0/L1) scenario. In the baseline scenario, the HTT will operate at the L0 input rate (1 MHz) and provide high quality tracks to the software High Level Trigger (HLT), operating as a co-processor, which will allow for a factor 10 reduction in the required size of the Event Filter (EF) CPU farm. The baseline Trigger and Data Acquisition (TDAQ) architecture is shown in Figure 1. In the evolved scenario, part of HTT is used in a low-latency mode (L1 Track), providing tracks in regions of the ATLAS detector at a rate up to 4 MHz. The main criteria for the evolved scenario are to keep the hadronic trigger rates and the occupancy of the inner pixel layers at adequate levels.

This note focuses on the baseline scenario. All the information and figures can be found in the ATLAS Phase-II Trigger and Data Acquisition Technical Design Report [2].

2. HTT system overview

The HTT system is an ATCA-based hardware implementation and is organized in independent HTT units. Each HTT unit is interfaced to the EF CPU farm via dedicated servers, HTT InterFaces (HTTIF). All boards are based on the same Tracking Processor (TP) motherboard and differ only by mounting different mezzanines. Each HTT unit contains 12 Associative Memory TPs (AMTPs) and two Second Stage TPs (SSTPs). The AMTP board mounts one Pattern Recognition Mezzanine (PRM) and the SSTP board mounts two Track Fitting Mezzanines (TFM). Figure 2 shows an overview of the HTT unit, including the TP boards and the connection with HTTIF.

The TP board is a high-bandwidth motherboard that can fit two small mezzanines or one large mezzanine. It is designed to host one large FPGA and 10 Gbps links. It is responsible for the communication to and from the HTTIF, for the data sharing and for specific algorithms such as pixel clustering and duplicate track removal. The firmware blocks for the TP boards have been designed and the demonstrator is expected by October 2019. Integration and cooling tests are planned to take place at CERN, starting in August 2020.

The PRM performs pattern matching using eight ITk layers. It takes as input ITk clusters and returns 8-layer tracks. It hosts four blocks of six AM-ASICs and one large FPGA (candidate Intel® Stratix® 10). The firmware development is ongoing and the demonstrator is expected by May 2020.

The AM-ASIC is the core component of HTT. It performs pattern matching between incoming data and pre-stored patterns. The production version of the ASIC will be called AM09. The current state of the art AM-ASICs are the ones used by the FTK system (AM06). In order to fulfill the HTT requirements, several improvements will be needed with respect to AM06. The prototype for AM07 is currently under test. The design for AM08 is already ongoing. AM09 is expected by 2021. It is expected to perform approximately 30 peta comparisons per second per chip and to be within the area and power consumption budgets.

The TFM extrapolates the PRM tracks to the remaining ITk layers and performs 13-layer track fitting. It takes as input the tracks from the PRM and the remaining ITk clusters and returns tracks with resolution close to offline. It hosts one large FPGA with high-speed links to the TP boards and the PRMs. The firmware development is ongoing and the demonstrator is expected by December 2019.

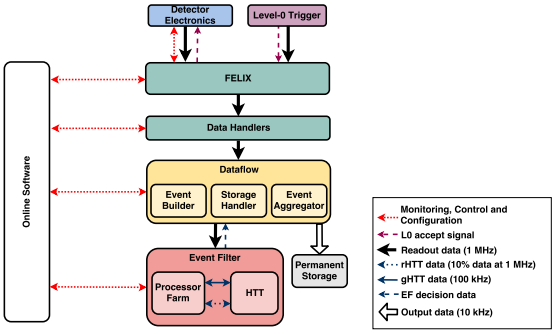

Figure 1: The main functional blocks of the baseline DAQ architecture for Phase-II [2].

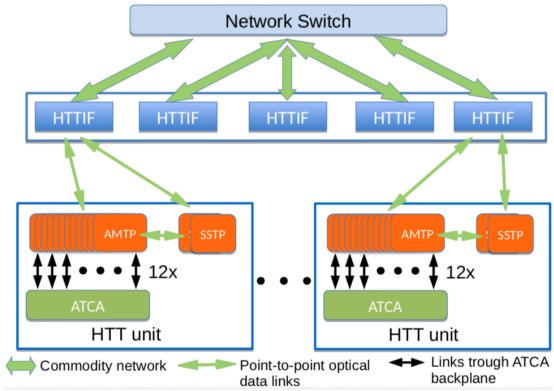

Figure 2: Overview diagram of the HTT system showing interconnections within HTT units and with the HTTIF [2].

3. HTT processing and expected performance

Depending on the trigger signature, two types of requests from the EF can be transmitted to HTT: finding tracks in regions of interest identified by the L0 trigger system (regional tracking, rHTT) or reconstructing tracks in the entire ITk coverage (global tracking, gHTT).

Regional tracking reconstructs tracks with $p_{\mathrm{T}} > 2$ GeV. It will operate at the full L0 rate and process data from about 10% of the ITk detector. For these tracks, single-stage reconstruction is performed using eight ITk detector layers. The rHTT will accomplish a significant reduction in the L0 rate, from 1 MHz to 400 kHz.

Global tracking reconstructs tracks with $p_{\mathrm{T}} > 1$ GeV at a nominal rate of 100 kHz. In addition to a first stage of track reconstruction, that is common to rHTT, a second stage of track fitting is performed, using all the 13 ITk detector layers, in order to provide high-quality tracks with better track parameter resolution.

The HTT processing proceeds as follows. The HTT inputs are ITk hits. There are two stages of processing, the first of which is common to rHTT and gHTT. The main operations are pattern matching, which is performed in the AM-ASICs, and track fitting, that is performed in FPGAs.

The first stage starts by clustering the hits from the eight ITk layers into consecutive ITk strip or pixel channels (referred to as superstrips). Then the superstrips are compared to a large bank of pre-computed patterns. This comparison is performed in the AM-ASICs. For each hit pattern that matches a template, the track parameters and quality are computed from the corresponding full-resolution hits in a FPGA. Tracks that share more than a given number of hits (duplicate tracks) are removed. After this stage, the rHTT tracks are complete and are transferred back to the EF.

During the second stage processing, which is performed only for gHTT, each 8-layer track fit is extrapolated to the remaining ITk layers and associated to any matching hits. A full track fit is then performed to achieve the best possible track parameter resolution. Duplicate removal is also performed. After this stage, the gHTT tracks are complete and are transferred back to the EF to be used in the final EF decision.

The resolutions of the d_0 track parameter for first- and second-stage fitting are shown in Figure 3 in red and blue, respectively. The resolution for offline fitting is also shown, in black. The first-stage track finding efficiency for muons with $p_{\mathrm{T}} > 4$ GeV is shown in Figure 4 for different η regions. The efficiency is close to 100% across the entire p_{T} range.

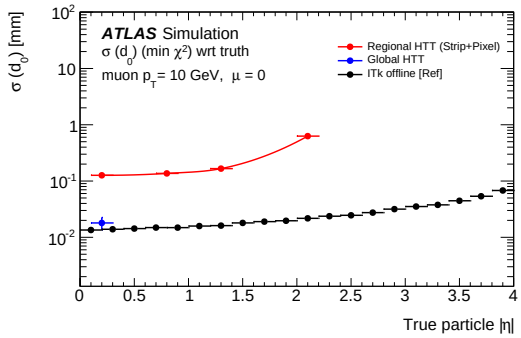

Figure 3: d_0 resolution for first- and second-stage fitting and offline [2].

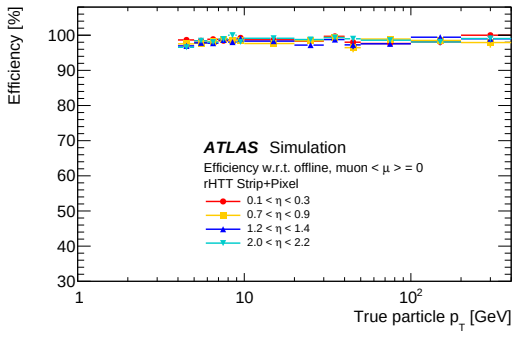

Figure 4: First-stage muon track-finding efficiency in η regions for muons with $p_{\mathrm{T}} > 4$ GeV [2].

4. Conclusions

The HTT system is the proposed solution for the ATLAS experiment to handle the challenging pileup conditions predicted for Run 4. It is a highly parallel system capable of performing track finding in hardware with short latency and a crucial part of the ATLAS detector upgrade for the HL-LHC.

References

[1] ATLAS Collaboration, Fast TracKer (FTK) Technical Design Report, (CERN-LHCC-2013-007. ATLAS-TDR-021), Jun 2013.

[2] ATLAS Collaboration, Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System, (CERN-LHCC-2017-020. ATLAS-TDR-029), Sep 2017.