PROCEEDINGS OF SCIENCE

CATIA: APD readout ASIC for CMS phase 2 ECAL electronics upgrade

P. Baron, M. Dejardin, O. Gevin[1], F. Guilloux[2] on behalf of CMS collaboration

IRFU, CEA, Université Paris-Saclay
F-91191 Gif Sur Yvette, France

E-mail: fabrice.guilloux@cea.fr

The incoming LHC upgrade to HL–LHC calls for a change of the ECAL front-end electronics design in order to maintain the present performance of the detector while facing a higher instantaneous luminosity and to optimize the timing resolution while using the existing crystals and APDs. The design of the new front-end electronics is based on the cascading of two ASIC: a fast, dual gain trans-impedance amplifier designed in a 130 nm CMOS process (named CATIA) and a dual ADC designed in a 65 nm CMOS process. The latest test–beam and laboratory test results of CATIA coupled with an ADC will be presented.

Topical Workshop on Electronics for Particle Physics
2-6 September 2019
Santiago de Compostela - Spain

[1] Speaker
[2] Corresponding author

PoS(TWEPP2019)001

1. CMS ECAL electronics upgrade

The High Luminosity Large Hadron Collider (HL–LHC) program foresees about one order of magnitude additional integrated luminosity with respect to the former LHC program over ten years. The impact of the increased luminosity has been carefully taken into account for the current Compact Muon Solenoid (CMS) Electromagnetic Calorimeter (ECAL) barrel detector: the main weakness of the readout electronics is the limitation of its bandwidth, as it will not be able to sustain the expected data flow [1]. In addition, the increase of the hit density leads CMS to adopt a new strategy concerning data selection through a Level 1 trigger. The data retention latency has been extended and the granularity has been enhanced by using the information from every single crystal [2].

The bandwidth limitation and the increase of Level 1 trigger latency have called for a complete redesign of the ECAL electronics and in particular the front-end electronics. The new ECAL electronics topology is designed for a continuous readout of the detector. The Level 1 trigger generation and buffering is moved to the back-end electronics. Fitting the continuous readout system, the proposed solution for the front-end electronics is a cascade of two custom Application Specific Integrated Circuit (ASIC): a trans-impedance amplifier (TIA) followed by an analog to digital converter (ADC). The TIA —named CATIA— is a fast, dual gain circuit designed in a 130 nm TSMC CMOS process. The ADC is a 12-bits, 160 Msps dual channel circuit implementing the gain selection and the data compression. It is designed in a 65 nm TSMC CMOS process (Figure 1).

After a first successful prototype in 2017, a full featured CATIA (V1) ASIC has been delivered in September 2018. The first section of this document presents the architecture of CATIA V1. The second section shows the latest results from the former prototype in a test-beam and from CATIA V1 in laboratory, in both cases driving an ADC as in the final setup.

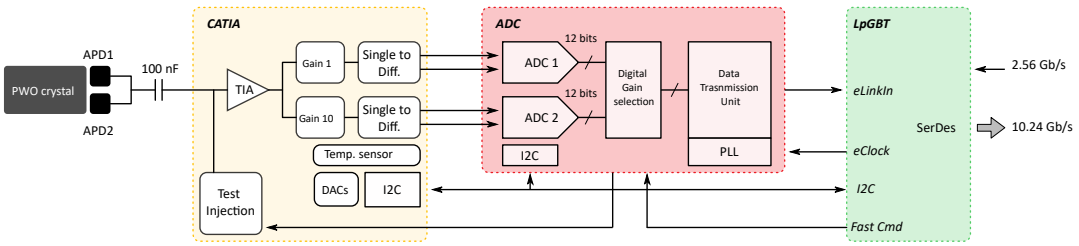

Figure 1: Cascade of ASIC to readout the CMS ECAL crystals. From left to right, the ASIC are a dual gain trans-impedance amplifier (CATIA), a dual ADC (Lite-DTU) and a digital concentrator (LpGBT).

2. CATIA V1

2.1 Required performance

In the incoming upgrade of CMS ECAL for HL-LHC, the particle sensitive $PbWO_4$ crystals, the avalanche photo diodes (APD) and the interconnection Kapton cables have not

been modified. They totalize an average of 200 pF of input capacitance and 90 nH of input inductance before the APD readout ASIC. The new front end electronics is expected to match the initial ECAL performance while mitigating the noise increase due to the radiation induced leakage current of the APD. Indeed, at the end of the HL-LHC program, the APD leakage current is foreseen to be up to 100 µA. The radiation increase also impacts the front end ASIC which needs to sustain up to 10 Mrad (safety margin included).

The current front end has a dynamic range from 50 MeV to 2 TeV (1.8 fC to 72 pC) with an integral nonlinearity below 0.2 %.

In addition to the former requirements, the front end ASIC has to provide a time resolution of 30 ps at the energy of 50 GeV. The timing resolution is used either to tag in time the incoming particles or to reject "anomalous signals". Indeed, unwanted signals are generated because of the direct interaction of particles in the APD silicon and should be discriminated from the scintillation signals. This could be achieved by signal shape recognition.

2.2 ASIC architecture

The CATIA ASIC is a single sensor readout system chip featuring two output channels, one for low energy (10 MeV-200 GeV) and one for high energy (10 MeV-2 TeV). The input stage relies on a Trans-Impedance Amplifier (TIA), based on a regulated common gate circuit using thick-oxide transistors and a 2.5 V power supply allowing to reach the linearity requirements. The input stage is followed by two channels with two gain stages: a by 10 gain for the low energy and a unity gain for the high energy measurements. Both gain stages are followed by an output differential buffer in order to drive the input stage of the sampling ASIC (ADC). The differential buffers include an internal 5-bit DAC to control the pedestal output voltage and an internal filter which reduces the signal bandwidth from 50 MHz to 35 MHz in order to fit to the bandwidth limitation from the Kapton cable. The output common mode could be externally set, allowing the use of an ADC supply voltage of either 1.2 V or 2.5 V.

Several testing functionalities in CATIA complete the analogue signal processing path: a 12-bits DAC coupled with a CMOS input pad is included to send to the TIA input a precise pulse for the linearity calibration. An analogue temperature sensor output—foreseen to be read out by the LpGBT internal ADC—is provided for temperature monitoring. All the internal registers of the ASIC are controlled by an I2C slave circuit with a custom Triple Modular Redundancy (TMR) architecture correcting single event upsets without the need of a continuous running clock.

3. Performance results

The first prototype of CATIA (V0) has been fully characterized in laboratory with results fulfilling the requirements and assessing the TIA design choice [1] [3]. The TIA and gain stages in CATIA V0 and CATIA V1 are almost identical.

3.1 Test-beam with CATIA V0

In addition to laboratory tests, beam tests have been carried with five CATIA V0 connected to ECAL crystals and APD, readout by a 160 Msps commercial ADC. As a whole, the test setup was representative to the ECAL experiment environment including the interconnect

cables and the power supply system. The temperature was set to 18°C. Results show that the energy resolution matches the legacy electronics and the time resolution meets the requirements (Figure 2 and Figure 3).

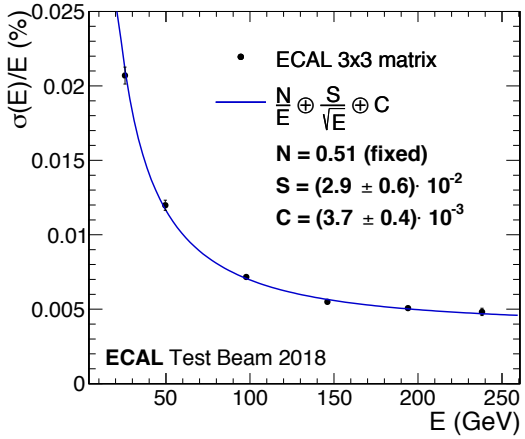

Figure 2: Energy resolution of CATIA V0 with a $PbWO_4$ crystal.

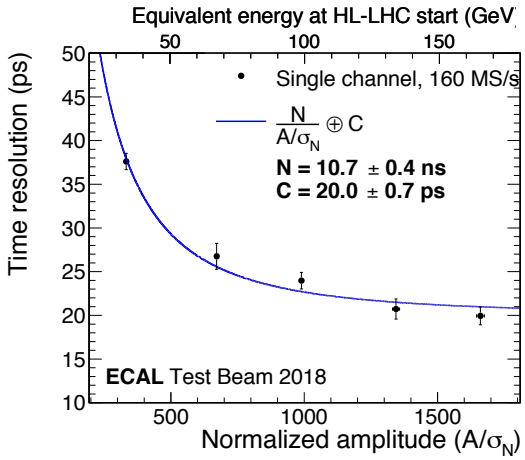

Figure 3: Time resolution of CATIA V0 with a $PbWO_4$ crystal .

3.2 Lab test with CATIA V1

The full featured ASIC was tested with two different data acquisition systems: first with a digital sampling oscilloscope in order to test the intrinsic performance of the TIA and the gain stages. A second test bench including a commercial ADC running at 160 Msps was used to investigate the performance of the TIA, the gain stage and the differential output buffers.

The noise measured at the output of the CATIA gain 10 channel with the internal filter set to 35 MHz was equivalent to an input referred current noise of 180 nA RMS. This is about 10 % higher than expected from the simulations (Figure 4).

The linearity was tested with a controlled laser and the internal 12-bit current DAC. The DAC is designed to inject current directly at the TIA input instead of the APD current. Both measurements gave an integral nonlinearity below ± 0.1 % proving that the internal DAC and the analog channel meet the requirements (Figure 5). The noise was also measured with a commercial ADC running at 160 Msps. The input current noise was then about 200 nA. The noise increase could be explained by the increased complexity of the test board holding the 5 CATIA and the 5 ADC, leading to a degradation of the TIA power supply and external voltage references environment. In addition, small glitches due to the ADC "sample and hold" circuit activity were observed. These glitches are signal amplitude dependent: when the differential signal is close to the pedestal value (i.e. $V_{diff} = \pm 0.6$ V), they are greater than when the differential signal is zero (i.e. $V_{diff} = 0$ V).

The impact of the ADC on the CATIA outputs can be filtered out by adding an external RC filter on the differential line (Fc = 125 MHz) between the two chips. The noise level with the extra filter is then 175 nA (target is 170 nA) but the signal rise time increases from 6.25 ns to 6.50 ns which is still good enough to meet the timing requirements (Table 1).

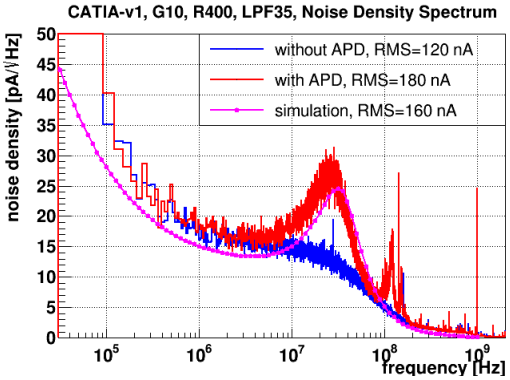

Figure 4: Noise spectrum of CATIA V1 from a digital sampling oscilloscope.

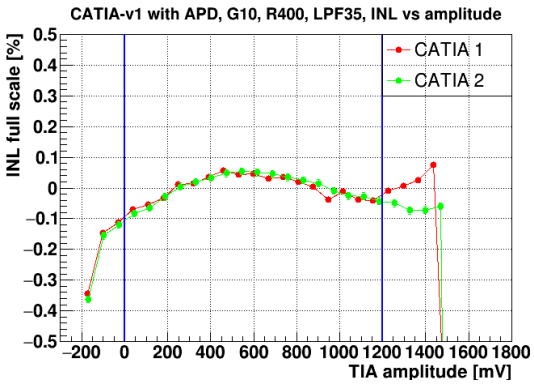

Figure 5: Linearity of CATIA V1 from a digital sampling oscilloscope.

Table 1: CATIA V1 lab results for gain 10 channel with internal low pass filter set to 35 MHz. DAQ : ADC@160 Msps.

Readout system	Noise (RMS)	Rise Time	INL
DSO	180 nA	6.25 ns	
ADC	200 nA	6.25 ns	± 0.1 %
ADC + Ext. Filter	175 nA	6.50 ns	

4. Conclusion

The technical choices of the CATIA ASIC architecture has been validated in laboratory and during the beam test: first on a prototype (CATIA V0) then on a full featured ASIC (CATIA V1). The performance results all match the expectations.

The next step is to validate CATIA in the final system (i.e. on the new VFE board) with the dual ADC specifically designed for CMS ECAL [4][5]. The key elements to check are the interfaces between the two ASICs (ADC inputs, shared I2C and, later on, calibration trigger generation) and the TIA sensitivity to the DC-DC converters. These final validations will lead to the final iteration of CATIA foreseen for the beginning of 2020.

References

[1] P. Baron, *The CMS phase 2 ECAL front end electronics upgrade*, poster in TWEPP 2018.

[2] F. Thiant, *New development in the CMS ECAL Level-1 triggersystem to meet the challenges of LHC Run 2*, in proceedings of TWEPP 2018 PoS(TWEPP-18)052.

[3] P. Baron, *Performance of CATIA ASIC*, in proceedings of TWEPP 2017 PoS(TWEPP-17)036.

[4] S. Commetti, *Design of the new front-end electronics for thereadout of the upgraded CMS electromagneticcalorimeter for the HL-LHC*, in proceedings of TWEPP 2017 PoS(TWEPP-17)106.

[5] S. Commetti, *The upgraded readout electronics of the CMS ECAL: system overview*, to be published in proceedings of TWEPP 2019.