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Design and test of current-mode DACs for threshold tuning of front-end channels for the High Luminosity LHC

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This work is concerned with the design and the characterization of digital-to-analog current converters, developed in a 65 nm CMOS technology, conceived for threshold tuning of front-end channels at the High-Luminosity LHC experiment upgrades. Two DAC structures were integrated in a small prototype chip, that was submitted in August 2018 in the framework of the RD53 developments. The prototype has been tested before and after exposure to X-rays up to a TID of 460 Mrad(SiO_2). The main performance parameters of the two structures are compared and discussed in the paper.

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1. Introduction

ATLAS and CMS tracker detectors at the High-Luminosity LHC (HL-LHC) will be equipped with low-noise pixel readout chips that are required to operate with very low stable threshold (of the order of 1000 electrons) and that will face unprecedented levels of radiation. In order to minimize the amount of noise hits at such low thresholds, it is vital that the analog front-end feature excellent performance from the standpoint of noise and threshold uniformity.
Pixel-to-pixel threshold variations in a multi-channel readout system (generally qualified in terms of threshold dispersion, i.e. the standard deviation of the threshold distribution) can be addressed by means of threshold tuning, a procedure during which the threshold of each pixel is locally adjusted with an in-pixel trimming digital-to-analog converter (TDAC).
This work is concerned with the design and the characterization of digital-to-analog current converters, developed in a 65 nm CMOS technology, conceived for threshold tuning of front-end channels at the HL-LHC experiment upgrades. Two TDAC structures were integrated in a small prototype chip, that was submitted in August 2018 in the framework of the RD53 collaboration [1].

2. Test structures

The main goal of the RD53 collaboration is the design of full-sized pixel readout chips for the ATLAS and CMS trackers at the HL-LHC [2], [3]. In August 2017 the collaboration submitted the RD53A chip [7], which includes a matrix of 400 $\times$ 192 pixels (half the size of the production chip) embodying three analog front-end designs called Synchronous, Linear and Differential. The prototype chip discussed in this paper integrates two standalone channels of the Linear front-end, each including a charge sensitive amplifier with Krummenacher feedback [4], a comparator and a TDAC for local threshold tuning. A more detailed description of the analog blocks integrated in the Linear front-end can be found in [5].
The prototype mainly serves the purpose of comparing two different TDAC designs (hereafter called design A and B), whose schematic diagrams are shown in Fig. 1. TDAC design A has been

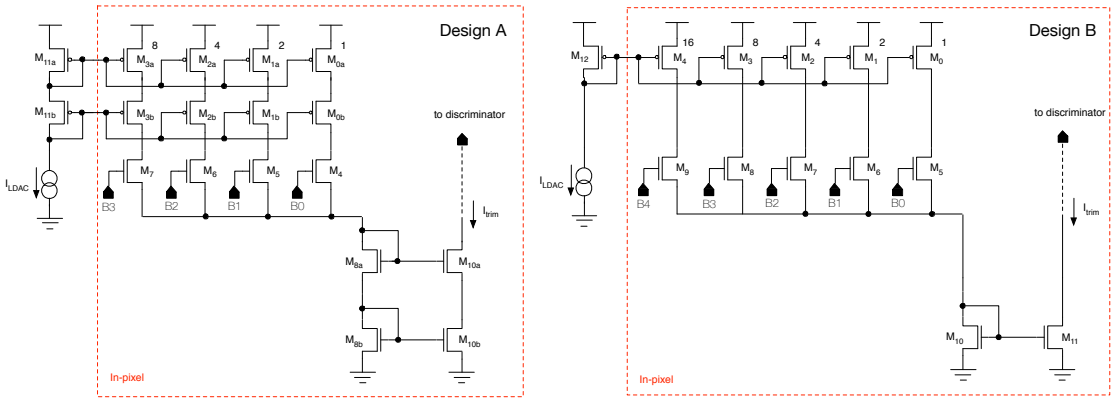

Figure 1: TDAC design A and B integrated in the prototype chip.

Table 1: Device size and polarity for TDAC design A and B.

	TDAC design A	
	Size[μm/μm]	Polarity[N/P]
M_{0a}, M_{0b}	0.5/3	P
M_{1a}, M_{1b}	1/3	P
M_{2a} M_{2b}	2/3	P
M_{3a}, M_{3b}	4/3	P
M4-M7	1/0.5	N
M_{8a}, M_{8b}, M_{10a}, M_{10b}	1/3.5	N
	TDAC design B	
	Size[μm/μm]	Polarity[N/P]
M_0	0.5/6	P
M_1	0.5/3	P
M_2	1/3	P
M_3	2/3	P
M_4	4/3	P
M5-M9	1/0.5	N
M_{10}, M_{11}	1/3.5	N

integrated in the RD53A Linear front-end, whereas design B has been conceived for the integration in full-sized production chips. Design A features a 4-bit, binary weighted current DAC with cascoded current mirrors laid out with no dummy transistors, whereas design B includes a more compact, 5-bit current DAC with the same binary weighted architecture, but with regular current mirrors. Dummy transistors have been integrated in the TDAC design B. The output current of the TDAC, I_{trim}, is connected to an internal node of the comparator. The lack of dummy transistors in design A is due to the limited amount of area for the integration of the analog blocks in the pixel cell, which also includes, in a 50 μm $\times$ 50 μm region, very dense logic circuits. On the other hand, the removal of cascode structures in the design B enabled the integration of an additional trimming bit in a reduced overall TDAC area. With respect to the RD53A version of the Linear front-end, integrating the TDAC design A, the additional bit in design B is expected to reduce the threshold dispersion across the pixel matrix in the production chip. Table 1 gathers device size and polarity for the two TDAC designs. PMOS current mirrors (M_{11a} and M_{11b} in design A and M_{12} in design B) are used as biasing networks out of the pixel region. The current generator I_{LDAC} has been implemented, in the prototype chip, by means of off-chip resistors, while additional current mirror stages fed by a current generated by a global, on-chip DAC will be integrated in the production chip. In the full-sized chip a maximum static voltage drop around 10 mV is expected on the power supply lines. Nonetheless, circuit simulations show that this effect has a negligible impact on the performance of both the designs of the TDAC.

3. Test results

TDACs performance has been evaluated in terms of dynamic range (threshold variation at the comparator input, simply computed as the difference between the threshold achieved for the maximum TDAC input code and the one obtained for TDAC code set to 0), integral and differential non-linearity (INL and DNL, respectively), for two different dynamic range settings. In particular,

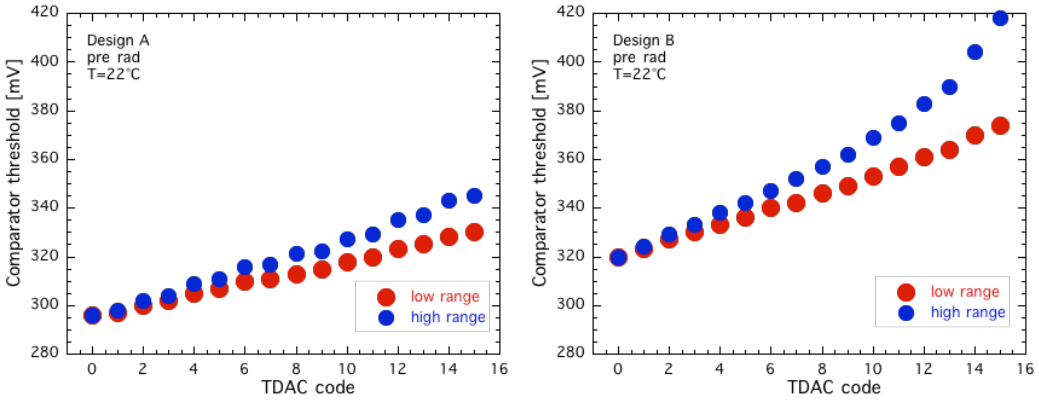

Figure 2: Input-output characteristics of TDAC design A (left) and B (right) operated in low (red circles) and high (blue circles) range modes. For the sake of the comparison with design A, 4 bits (out of 5) have been exploited for TDAC design B.

TDACs were operated in low dynamic range mode (I_{LDAC} set to 12 μA) and high dynamic range mode (I_{LDAC} set to 17 μA). A least significant bit (LSB) current of 38 nA and 53 nA has been obtained from circuit simulations for the design A operating in low and high dynamic range mode, respectively (24 nA and 33 nA for TDAC design B). For the sake of the comparison with design A, 4 bits (out of 5) have been exploited for TDAC design B. The performance of the two TDACs has been assessed before and after exposure to total ionizing doses up to 460 Mrad(SiO_2) of X-rays, with a dose rate of 3.1 Mrad(SiO_2)/h.

3.1 Pre-irradiation results

Fig. 2 shows the comparator threshold as a function of the TDAC code for design A and B operated in both low (red circles) and high (blue circles) range mode. It is worth noticing that an output dynamic range around 50 mV can be achieved for design A in high range mode and design B in low range mode. In the following, INL and DNL will be compared for these particular settings, where the dynamic ranges of the two TDAC designs are almost identical. Two different kinds of non-linearities have emerged from the test. The first one, clearly noticeable for TDAC design A, has to be related to the lack of dummy transistors in the layout of the current DAC. The PMOS transistors M_{0a} and M_{0b} (Fig. 1), controlled by the least significant bit B0, are indeed laid out at the boundary of the TDAC structure and well proximity effects [6] are thus not minimized, resulting in different LSB step heights for even and odd codes. The second one can be detected for TDAC design B operated in high range mode. In this configuration, the value of the DAC output current, I_{trim}, can approach the quiescent current of the comparator input stage, resulting in a significant non-linearity for higher TDAC codes. The INL and DNL are shown in Fig. 3 as a function of TDAC code for design A operated in high range mode and design B operated in low range mode. Both the designs feature a DNL smaller than $\pm$1 LSB with monotonic input-output characteristics, with a maximum INL slightly exceeding 1 LSB for TDAC design A.

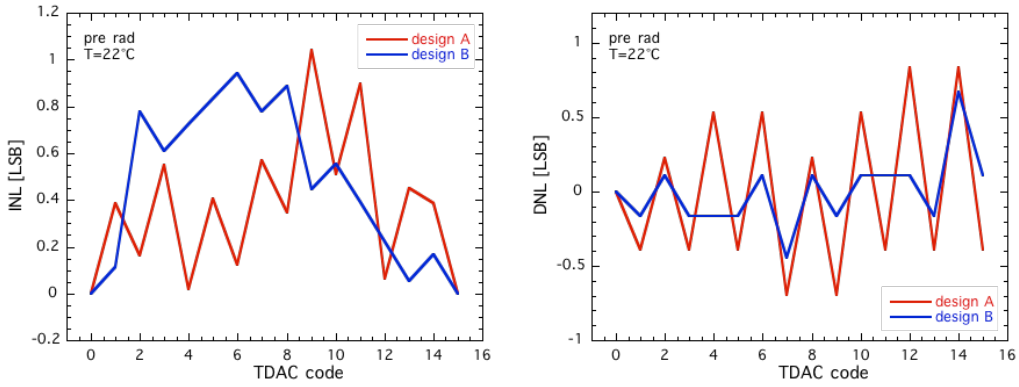

Figure 3: INL (left) and DNL (right) for TDAC design A operated in high range mode and design B in low range mode.

3.2 Post-irradiation results

Fig. 4 shows the comparator threshold as a function of the TDAC code before irradiation and after exposure to TIDs of 1, 85 and 460 Mrad(SiO_2). The figure also reports data obtained after 48 hours annealing at room temperature. TDAC input-output characteristics are slightly affected by radiation for doses up to 85 Mrad(SiO_2), whereas non negligible effects can be detected for both the designs at the highest dose. In particular, two major effects take place at this radiation level: an increase of the output dynamic range and a shift in the absolute value of the comparator threshold. It is worth mentioning that the actual threshold depends not only on the value of the I_{trim} current, which can be adjusted by changing the TDAC input code, but also on the transconductance of the comparator input stage (implementing a classical NMOS differential pair with PMOS active load), which should be constant. The variation in the dynamic range can be ascribed to a reduction, after the irradiation, of the current biasing the comparator input stage, resulting in a smaller transconductance of the stage and, in turn, in a larger threshold dynamic range. The dynamic range of

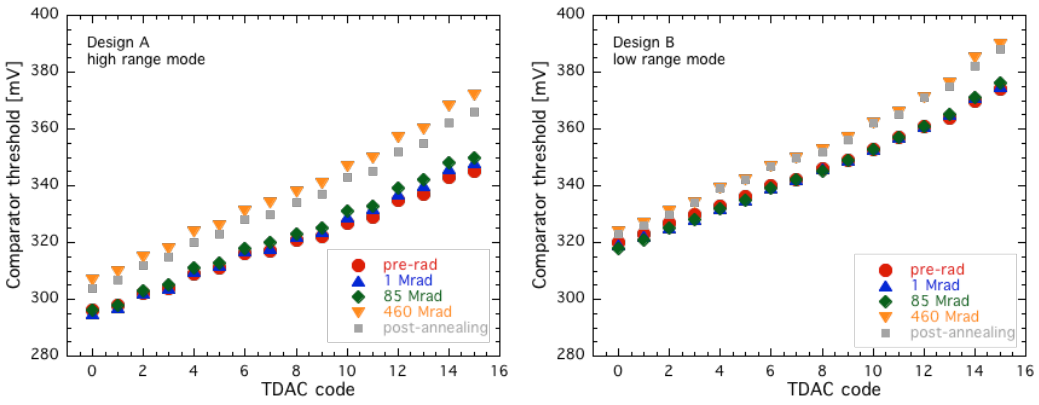

Figure 4: Input-output characteristics of TDAC design A (left) and B (right) at different TIDs. TDAC design A operated in high range mode, design B in low range mode.

TDAC design A and B before irradiation is equal to 49 mV and 54 mV, respectively, with an increase of 33% (design A) and 22% (design B) at 460 Mrad(SiO_2). The threshold shift looks more pronounced for design A, with an increase of the absolute threshold close to 11 mV for TDAC code set to 0.
The threshold dispersion properties of the Linear front-end have been investigated by means of a purposely developed simulator, written in Python and not discussed in this work. Such a simulator combines the data obtained from the characterization of the TDAC design A and B, and the untuned threshold dispersion data coming from the test of the RD53A chip. The simulation results point out that both the TDAC designs make the front-end compliant with the threshold dispersion specifications set by the experiments, also after irradiation.

4. Conclusions

A prototype chip including two standalone channels of the RD53A Linear front-end was submitted and tested with the aim of comparing two different threshold trimming DAC designs. The performance of the two DACs has been evaluated before and after the exposure to total ionizing doses up to 460 Mrad(SiO2). Both the designs are fully functional after irradiation, with a non-negligible increase in the DAC output range and a threshold shift detected at the highest radiation level achieved during the irradiation campaign. Nonetheless, one of the two designs (namely TDAC design B) features a larger dynamic range and higher degree of tolerance to ionizing radiation and will be the preferred option in view of operation in the threshold tuning system of a full-sized pixel detector readout chip at the HL-LHC.

5. Acknowledgements

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