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A SiPM readout front-end with fast pulse generation and successive-approximation register ADC

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A low-power front-end with on-chip fast pulse generation and customized 10-bit single-ended SAR ADC is developed for SiPM readout design. The on-chip fast pulse generation improves the timing resolution without the need of extra I/O pins. The proposed SAR ADC, reusing the SiPM charge integrator and eliminating the power-hungry charging sensitive amplifier, consumes significantly less power compared with conventional solutions. Designed in a 0.18 µm 1P6M bulk CMOS technology, the front-end contains 16 channels of SiPM readouts, and each channel consumes a power of 3.8 mW. With on-chip HPF to shape input signals, the fast pulse generation approach reduces the long-tailed SPE pulses width from 50 ns to 3 ns. At 16 MS/s, the SAR ADC consumes 743 µW from a 1.8 V supply and achieves a SNDR of 57.53 dB and a SFDR of 66.31 dB, respectively.

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1. Introduction

ASICs for silicon photomultiplier (SiPM) readout with high timing resolution and low power consumption are required for high-energy physics experiments. However, the large quenching RC time constant of SiPM cause a much longer tail in the single photo-electron (SPE) response. As the output current pulse of SiPM is formed by hundreds of SPE responses from triggered microcells, the current pulse is therefore shaped with a slow rising edge. The slow rising edge of the current pulse makes the timing measurement to be sensitive to the noise of the readout electronics. To address the issue, SensL [1] has developed a modification to the standard SiPM structure that results in a third terminal carrying an ultra-fast output signal. In the modified structure, by adding a small capacitor in parallel with the quenching resistor in each microcell, a high-frequency output path is established from the standard path. Nevertheless, the drawback of the SensL's approach is obvious. As both the fast and standard outputs are required, the input pin counts of the readout ASIC are doubled, which results in a costly and cumbersome design, especially for applications where thousands of SiPM detectors and readout circuitries are needed. In terms of energy measurement, the conventional SiPM readout ASIC often utilizes a power-hungry charge sensitive amplifier (CSA) to integrate the scaled current onto an integration capacitor, and a low speed Wilkinson ADC is then employed to digitize the CSA output voltage. Such an approach unfortunately suffers from high power consumption. The high power dissipation also inevitably leads to a high working temperature, which can cause SiPMs to generate more dark count noises, deteriorating the timing and energy measurement accuracies. Low-power SiPM readout ASIC is required for systems with a large amount of SiPM detector arrays, especially for low temperature experiments (like liquid argon dark matter program).

In this paper, we report a 16-channel SiPM front-end with high timing resolution, low I/O pin counts and low power consumption. An on-chip high-pass filtering approach is adopted to generate the fast current pulse from the standard output of SiPM without the need of extra I/O pins. The fast current pulse significantly helps to improve the timing measurement accuracy. To achieve low power consumption, a customized 10-bit SAR ADC directly digitizes the output voltage of the charge integrator in each channel by reusing the charge integration capacitor as the sampling capacitor. Besides, benefiting from the high sampling rate of the SAR ADC, the readout system uses a single SAR ADC that is shared among the 16 channels for energy digitization, which provides a compact design with much lower power consumption.

2. Readout architecture and circuit designs

2.1 Readout architecture

Fig. 1 shows the block diagram of the proposed SiPM readout ASIC and its timing diagram. In the diagram, a standard current pulse is generated at time T_0, and is then duplicated by the current mirror and sent to an on-chip high-pass filter (HPF) for fast current pulse generation. The generated fast pulse then triggers the current discriminator at time T_1 (regarded as the pulse arriving time). After that, the output of the current discriminator triggers the timing stamp pulse and also enables the switch $S_{1,N}$ to start the charge integration process with a scaled input current pulse onto the charge integration capacitor $C_{Q,N}$. After an integration time period of

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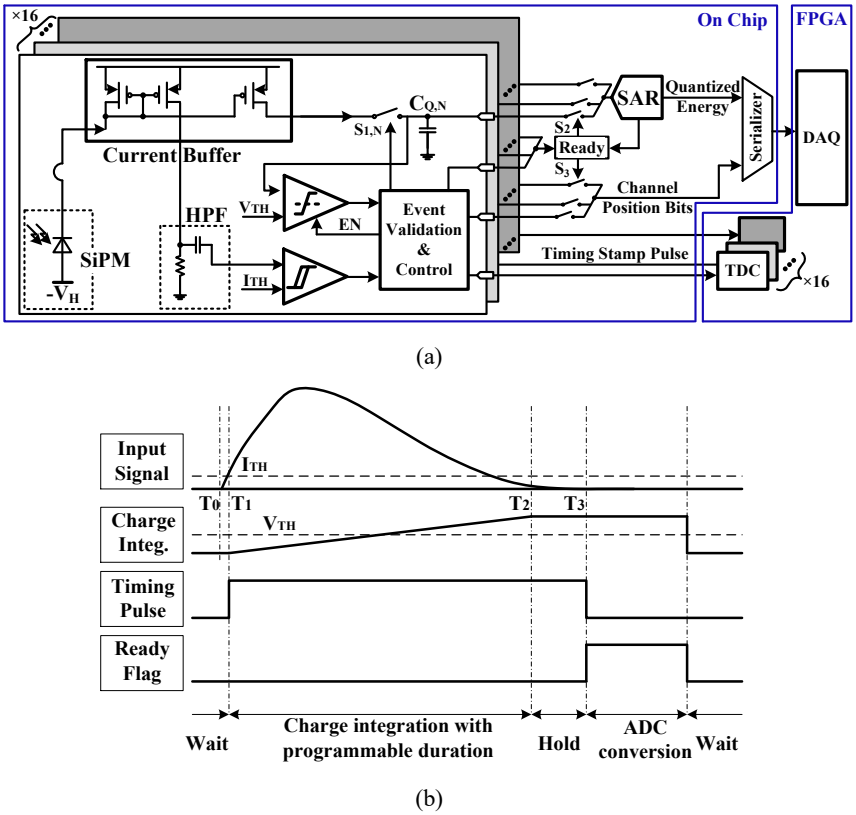

Fig. 1. (a) Block diagram of the proposed 16-channel SiPM readout and (b) its timing diagram.

ΔT, which is programmable depending on the amplitude of the input current strength, $S_{1,N}$ will be switched off and the voltage discriminator will be enabled by a control signal at time T_2. By comparing the integrated voltage on $C_{Q,N}$ with a predefined threshold voltage V_{TH}, the voltage discriminator makes a decision as whether the event is a true photon event or is or a false event caused by dark count noise. If it is decided that the event is a false event, $C_{Q,N}$ will then be discharged immediately. Otherwise, a ready flag signal will enable the switch S_2 to start the digitization of the integrated voltage on $C_{Q,N}$ for energy measurement at time T_3. The switch S_3 will also be enabled by the ready flag signal to transmit the channel position information to an on-chip serializer. At T_3, by flipping down the timing stamp pulse, the ready flag signal will also inform the off-chip FPGA-based time-to-digital converter (TDC) system to start the digitization of the timing pulse from T_1 to T_3. With the knowledge of the timing pulse length and time point T_3, the FPGA-based data acquisition (DAQ) system can then determine the signal arriving time T_1 to acquire the timing information of the SiPM photon event.

2.2 Current buffer with on-chip HPF

The output impedance of the SiPM detector is finite since each SiPM detector is composed of thousands of microcells in parallel connection, therefore a readout circuit with low input impedance is essential to achieve high bandwidth to prevent significant loss of the SiPM output currents. Comparing with voltage-mode readout structure, current-mode input buffer can conveniently provide a lower input impedance [2]. In Fig. 2, a simplified schematic of the input current buffer with the on-chip HPF is depicted. By inserting a common gate NMOS transistor between the input node and the current mirror and adopting a current feedback topology through transistor M_{P2}, the input impedance of the current buffer can be further reduced by a factor of N

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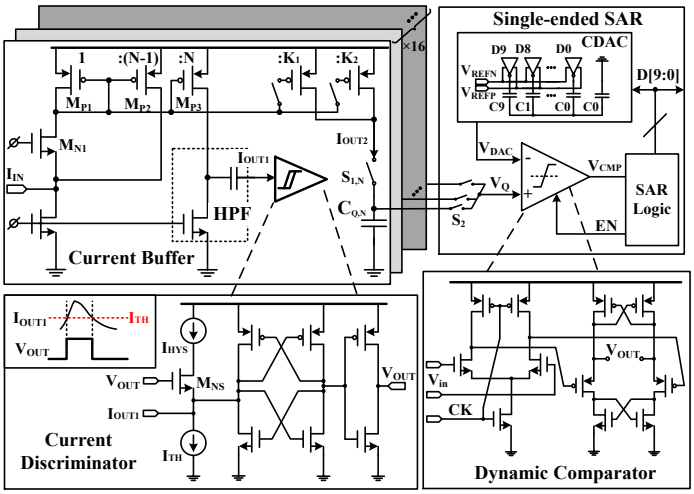

Fig. 2. Current buffer with on-chip HPF, SAR ADC and current discriminator with enhanced stability.

[3], where N is the current mirror ratio. With a 1:1 scaling factor, a copy of the input standard pulse is then outputted to the on-chip HPF to generate the fast signal pulse I_{OUT1}. Depending on the amount of the input charge, a scaled current pulse I_{OUT2} will be integrated by $C_{Q,N}$ as soon as the current discriminator is triggered.

2.3 Customized SAR ADC

The schematic of the 10-bit single-ended SAR ADC is also shown in Fig. 2. Different from the typical implementation of SAR ADCs, where the capacitive DAC (CDAC) is reused as the sampling capacitor during the sampling phase, the proposed ADC sampling capacitor is designed by directly reusing the SiPM integration capacitor $C_{Q,N}$, and is separated from the CDAC. Benefiting from this modification, the size of the sampling capacitor is no longer dictated by the matching requirement of the CDAC. Instead, the sampling capacitor can be sized mainly based on the signal-to-noise ratio requirement. Also, the power hungry CSA is avoided. The proposed SAR ADC mainly consists of a dynamic comparator, a CDAC, and a SAR logic block with a synchronous clock generation circuit. With the ready flag from the control logic enabling the switch S_2, the SAR ADC will start to digitize the voltage integrated on $C_{Q,N}$. The SAR ADC output is combined with a 4-bit channel position bits, allowing the 16 channels to share a single SAR ADC. The combined output is then sent to the on-chip serializer, which provides the final energy digitization outputs to the DAQ system.

3. Simulation results and analysis

The 16-channel SiPM readout is designed in a standard 0.18 µm 1P6M CMOS process. Fig. 3 shows the transient responses of two adjacent channels of the 16-channel readout ASIC, which are consistent with the timing flow as shown in Fig. 1 (b). Both the on-chip fast pulse generation and the SPICE model of SensL's SiPM with fast output [1] are investigated. As shown in Figs. 4, the proposed approach achieves similar single photo-electron responses comparing with those of the SensL's SiPM fast-pulse model. By shortening the long-tailed single photo-electron from 50 ns to 3 ns width, a 30 ps timing resolution improvement can be achieved [1]. At a sampling rate of 16 MS/s, the proposed single-ended SAR ADC consumes only 743 µW from a 1.8 V supply, and achieves a SNDR of 57.53 dB and a SFDR of 66.31 dB,

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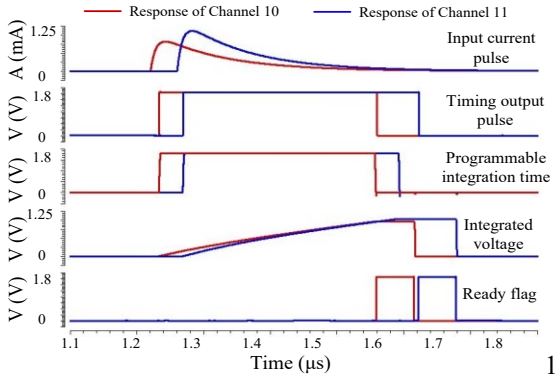

Fig. 3. Transient responses of two adjacent channels of the proposed SiPM readout.

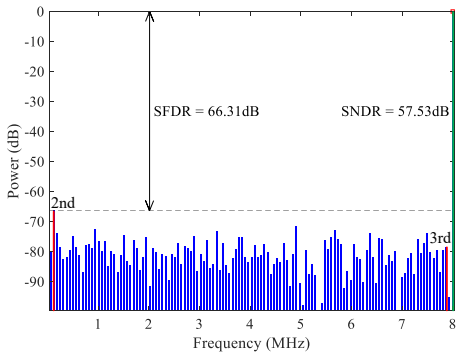

Fig. 5. ADC output spectrum at 16 MS/s sampling rate with a near-Nyquist input signal.

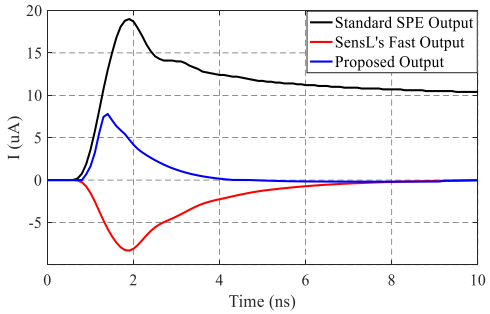

Fig. 4. SPE responses of the on-chip HPF and SensL's SiPM model.

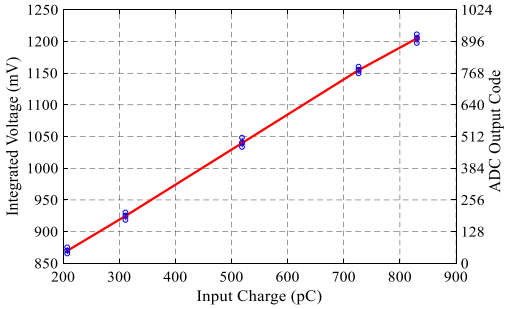

Fig. 6. ADC output codes versus different input charges among 16 channels.

respectively, as shown in Fig. 5. The ADC output codes corresponding to different input SiPM charge levels among the 16 channels are shown in Fig. 6, which presents good linearity for charge integration and digitization.

4. Conclusion

A current-mode low-power 16-channel SiPM readout ASIC with on-chip fast pulse generation and shared SAR ADC is developed. The on-chip fast pulse generation approach helps to improve the timing resolution without the need of extra I/O pins. By reusing the SiPM charge integrator as the sampling capacitor in the SAR ADC and eliminating the power hungry charge-sensitive amplifiers, the SiPM readout ASIC consumes 3.8 mW of power per channel. The shared SAR ADC not only reduces the area but also helps to further lower the power consumption. The proposed on-chip fast pulse generation and shared SAR ADC solution facilitates multi-channel SiPM readout designs with high timing resolution, low I/O pin counts and low power consumption.

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