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A Monitoring 12-bits Fully Differential Second Order Incremental Delta Sigma Converter ADC for TimePIx4

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This paper presents a 12-bits second-order incremental sigma delta converter for TimePix4 fabricated in a 65nm CMOS process. It does not need calibration and is robust to process variations because most of the signal processing is performed in the digital domain. It provides a maximum conversion rate of 1kSample/s, enough for monitoring the internal signals of the chip, consuming only 8µW. Simulations show a SNR of 84.9dB operating in free-running mode.

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1. Introduction

Delta-sigma converters offer high resolution at moderate speeds and present low sensitivity to process variations because a significant amount of the signal processing is performed in the digital domain. This robustness to process variations is an important feature nowadays, where the use of deep submicron processes is generalized and parameter spread is more significant in each new technological node. However, delta-sigma converters are not suitable to measure DC signals. In those cases, incremental delta-sigma converters, which can be considered delta-sigma data converters in transient mode, are used because they can be reset and easily multiplexed among several channels.

Incremental delta-sigma converters are a subclass of ΔΣ converters. The main differences are that they are operated during *n* clock cycles and with DC signals. The last condition is easily achieved with the use of a sample and hold at the input. Like ΔΣ converters, incremental converters have different architectures. The simplest one is a first order converter formed by an integrator and a comparator [1]. Its main drawback is a long conversion time because 2^{nbits} clock cycles are required to perform a conversion, like Wilkinson converters. The conversion rate can be improved by increasing the order of the converter and replacing the comparator by a DAC of *l* levels. A good matching in the DACs is needed because the quantization errors of the DAC are added to the total error of the converter [2]. Another way to increase the conversion rate, among others, is creating higher order modulators by cascading integrators. There are several types of cascaded architectures, but Cascaded-Integrators Feed-Forward (CIFF) architecture is one of the most used because is less sensitive to non-linearity of the integrators, has less voltage swing at the output of the integrators, and only one feedback DAC is needed. In addition, the Signal Transfer Function is 1. The operation of CIFF incremental ΔΣ converters is described in [1].

This paper presents a 12-bit delta-sigma ADC for monitoring bias signals instead of the common SAR solution, which requires a calibration circuit to achieve that level of resolution. This presented ADC is implemented inside TimePix4 and its purpose is to monitor 32 internal bias voltages. These are DC signals, so a sampling rate of 1ksample/s is enough. The chip has been designed in a 65nm CMOS process.

2. Architecture overview

A block diagram of a second order CIFF incremental sigma-delta converter is shown in figure 1. Coefficients a_i of the feed-forward paths are used to control the zero-poles of the Noise Transfer Function (NTF) while the coefficient c_i must be adjusted to avoid overflow at the output of the integrators. A binary DAC with values V_{ref} and $-V_{ref}$ closes the loop. The sigma-delta operates in such a way that the closed loop tries to balance the average value of the comparator *d* with the input value V_{in}. After *n* clock cycles and assuming V_{in} constant one gets:

$$\frac{V_{in}}{V_{ref}} = \frac{2!}{(n-1)n}\sum_{l=0}^{n-1}\sum_{k=0}^{l-1} d_k + e \qquad (1)$$

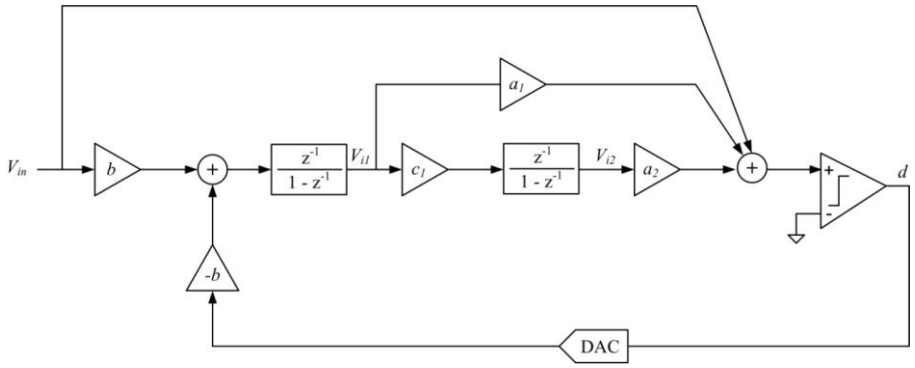

Figure 1: Block diagram of a 2nd order CIFF incremental delta sigma converter.

where *e* is the quantization error of the converter and d_k is a stream of 1s and 0s generated by the comparator which has to be processed by a digital filter to recover a digitalized value. The coefficients of the converter where determined by simulation.

The design of the ADC started by working at architectural level with Matlab. This allowed to determine the oversampling ratio, the open gain and band-width of the operational amplifiers, as well as to dimension the sizes of the capacitors. Instead of creating Simulink models for each integrating stage, it was used the SimSides library for Matlab developed by IMSE-CNM to design delta-sigma converters [3]. It was found that a second order Cascaded Integrators Feed Forward (CIFF) architecture operating with an oversampling rate of 210 allowed to meet the requirements in terms of conversion speed, area and power consumption. The different circuits of the converter were designed to work with a maximum oversampling frequency of 250kHz which produces a conversion rate of 1190samples/s.

Figure 2 shows a block diagram of the ADC. The phases of the first integrator stage were modified in order to work with single-ended input signals and provide a fully differential output for the fully differential second stage. The operational amplifiers are fully differential folded cascode with a switched-capacitor circuit to generate the common-mode voltage. With the 65nm

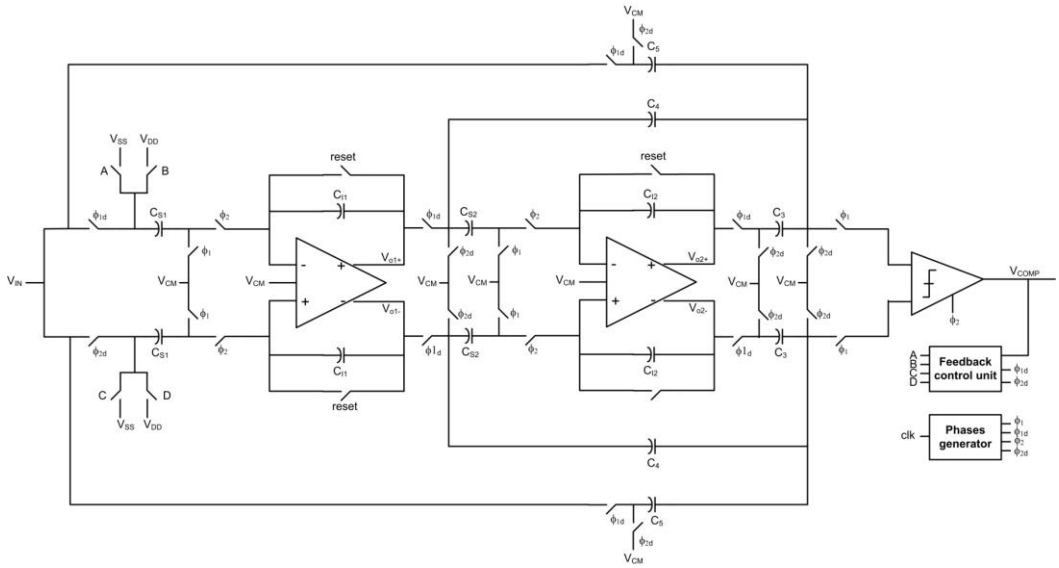

Figure 2: Conceptual schematic of 2nd order CIFF incremental delta sigma converter.

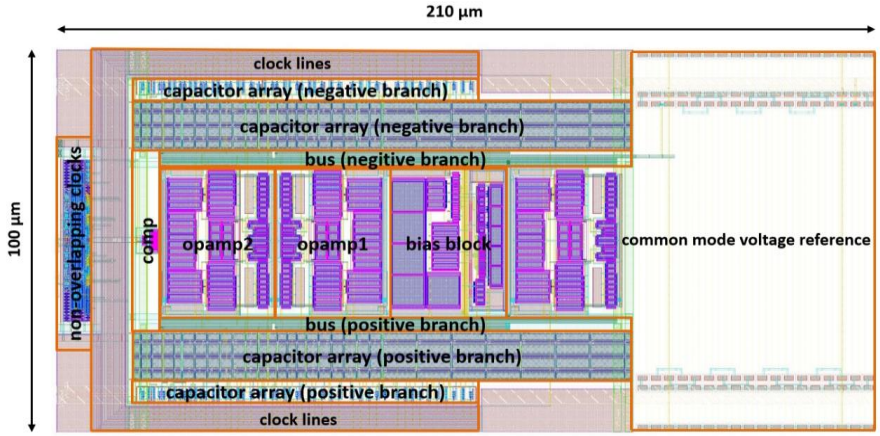

Figure 3: Layout of the 2nd order CIFF incremental delta sigma converter.

process, it was not possible to reach an open-loop gain of at least of 75dB as needed, so gain-boosting techniques were used to enhance the gain to 90dB. A SR dynamic latched comparator is used because fulfils the requirements in terms of speed and has DC zero current during the reset phase. The non-overlapping phase generator consists of a feedback loop made up of two NAND gates, each connected in series with a cascade of inverters. The voltage common mode reference V_{CM} is generated with a voltage divider composed of a voltage follower acting as a buffer. This is not depicted in figure 2.

The power consumption of the converter at an operating oversampling frequency of 250kHz is of 8µW working at 1.2V. This value includes the power consumption of the V_{CMR}. If this is not taken into account, the total power consumption of the modulator is of only 3.5 µW. A lot of care was taken in the layout to avoid crosstalk between signals that could degrade the performances of the ADC. The size of the layout of the modulator is of 150x110µm^2 and it is shown in figure 3. With the common mode voltage reference circuit, the size is increased to 210x110 µm^2. The filter is not shown in the figure because it was synthesized with the rest of the digital electronics of the chip.

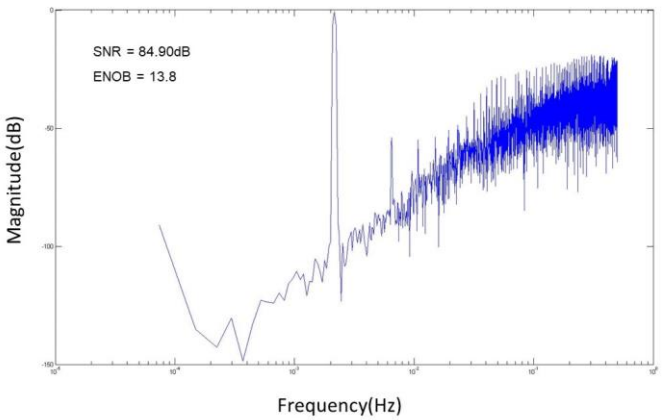

Figure 4: Output spectrum of the ADC.

3. Simulation results

The correct operation of the ADC was tested by simulation first at transistor level and latter at layout level. It was first checked working as a conventional delta-sigma converter, in the so-called free-running mode. The output spectrum to a 1.1V peak-to-peak and 543Hz sinusoidal waveform of a layout level simulation is depicted in figure 4. 210*64 samples were used to calculate the FFT. A SNR84.9dB was obtained in the typical process corner. This improved to 89.2dB for the best case and got worse to 80.4dB for the worst case.

The converter was also simulated working in incremental mode. However, the test of the whole range would have required a week at schematic level. It was decided to only check small regions of the whole range for all corners at schematic and layout level. Results shown that ADC achieved the desired resolution for an input range of 25mV-1175mV. Figure 5a shows the response of the ADC to different input values from 6V to 6.020V for 5different corners at schematic level. Figure 5b shows the INL for the same input range. It can be seen that the response of the ADC is robust to process variations.

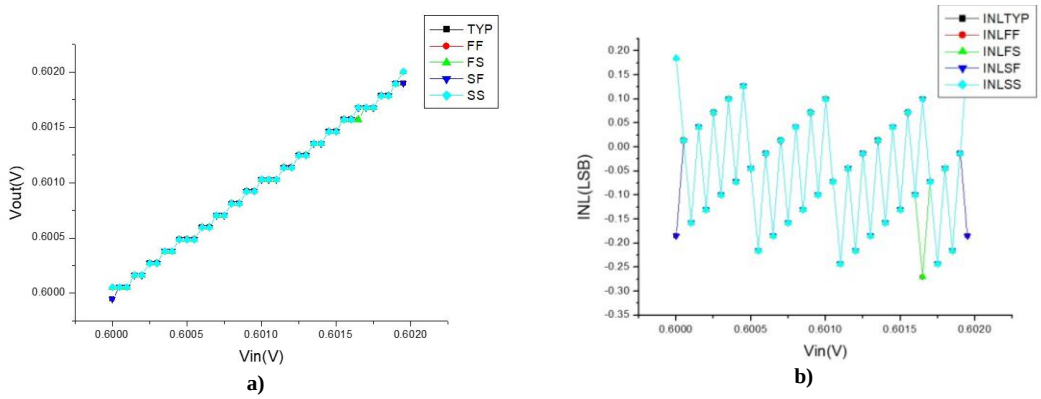

Figure 5: Simulated transfer curve **a)** and INL **b)** of the ADC for 5 differnent corners at schematic level. Robustness of the ADC against process variations is shown.

Conclusions

This paper has presented a 12-bits incremental delta sigma converter for monitoring several bias voltages of the TimePix4 chip. The ADC is robust to process variations because most of the signal processing is carried out at the digital domain. Therefore, no calibration circuit is needed. The delta sigma modulator has been optimized for low power, consuming only 3.5µW at an oversampling frequency of 250kHz for a sampling conversion of 1kSamples/s. It has a dynamic range of 1.1V.

References

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