## DECAL: A Reconfigurable Monolithic Active Pixel Sensor for use in Calorimetry and Tracking

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In this paper we describe the DECAL Monolithic Active Pixel Sensor (MAPS) for digital electromagnetic calorimetry. The sensor consists of a matrix of 64x64 55um pixels, and provides a readout at 40MHz of the number of particles which have struck the matrix in the preceding 25ns. It can be configured to report this as a total sum across the sensor (equivalent to the pad of an analogue calorimeter) or the sum per column (equivalent to a traditional strip detector). Design and operation of the sensor is described, and the results of chip characterisation are reported and compared to simulations.

Keywords—CMOS Image Sensor, configurable, calorimetry, tracking

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#### 1. Introduction

Calorimetry is an important technique for the determination of the energy of incident particles in an experiment. A small fraction of electromagnetic calorimeters are silicon-based devices, with the largest example under construction [1], and use layers of a dense, high atomic number, absorber material (such as lead or tungsten) interleaved with silicon as the detecting material. Particles incident on the absorber initiate showers of lower energy particles, which deposit energy in the detecting layers. The total charge deposited in each detector layer is then summed and read out. By performing this operation for each detector layer, the energy of the initial particle can be estimated.

However, it has been suggested that a digital approach can lead to higher energy resolution [2] and potentially take better advantage of low cost commercial imaging sensor technologies. In contrast to an analogue calorimeter, which sums the total deposited energy in a given detector volume, a digital electromagnetic calorimeter is segmented and counts the total number of particles passing through the volume.

In this paper, we describe DECAL, a Monolithic Active Pixel Sensor (MAPS) prototype designed for use as both a digital calorimeter and tracker.

#### 2. Application and Specifications

As described in the introduction, the overall goal of the DECAL sensor is to provide a count of the number of interacting particles over a given area. This value must be delivered for every bunch crossing, so the sensor must be capable of calculating and outputting this value at the LHC interaction frequency – i.e. every 25ns (40MHz).

As well as providing a complete count of hits over the sensor (referred to as "Pad Mode"), the sensor should be capable of operating as a strip sensor for tracking, by instead providing the total number of hits in a column ("Strip Mode").

For both modes, the input referred noise should be <80e- to allow detection of a 500e- signal. Maximum numbers of hits per column have been calculated for both modes based on expected hit density in a calorimeter coping with incident energies up to the multi-TeV range. Overflow flags should be provided if these values are exceeded. The maximum hits per column for Pad and Strip modes are respectively 15 and 3.

#### 3. Sensor Overview

In this section we provide a description of the sensor design and circuitry created to meet the requirements of the previous section. Figure 1 shows an outline of the sensor, which, as previously stated, can either operate in pad mode for a calorimetry application or in strip mode for a tracking application.



Figure 1 Overview of the sensor architecture, (a) Pad configuration and (b) Strip configuration

#### 3.1 Pixel

The front-end of the pixel is composed of a common-source amplifier as a preamplifier, followed by a cascoded common-source amplifier configured as CR-RC shaper for noise reduction. The diode is capacitively coupled and biased using a large resistance in order to allow high reverse bias voltages to be applied for the largest possible depletion region. Constant current feedback is used to bias the input to the preamplifier. Figure 2 shows the pixel architecture.

The output of the shaper is connected to a comparator to determine whether input signals have crossed the detection threshold. Before reaching the comparator, it is passed through the capacitor C5 whose bias is set by an in-pixel biasing DAC. This allows for pixel level correction of the threshold to compensate for variations in the shaper DC level and comparator offset.

The output of the comparator is then sampled by a global 40MHz clock "arrayClk". After this, the digital part of the pixel is automatically reset in order to be ready for the next beam crossing.



Figure 2 Overview of the architecture of the pixel.

#### 3.2 Column level summation

For each cycle, the number of hits in a column is summed and provided to the periphery within the next 25ns sampling period. This is done using asynchronous logic embedded between pixels. Figure 3 shows the logic used to sum groups of pixels from the same column. This process continues until a block of 8 pixels has been combined. Further addition of pixels proceeds in a sequential fashion, adding blocks of 8 until 64 pixels are summed at the bottom of the column.

The full summation operation is asynchronous and its speed is determined by the logic propagation delay, the full summation has therefore been designed to be shorter than the 25 ns.

Each column can add its total number of hits up to a maximum of 15. If the sum exceeds 15, the column sets an overflow flag.

#### 3.3 Periphery summation and reconfigurablility

The purpose of the peripheral circuitry is to either sum the hits and overflow bits and output 2 numbers (pad mode), or to provide the total number of hits for each column (strip mode). In strip mode, the total number of hits per column is limited to 3 to keep within the available output bandwidth.

Figure 4 shows how the peripheral logic is arranged. The chip is broken into 16 column sections, each with 4 LVDS output pads. In pad mode, sums and overflows are added to give 2 total values which are transmitted as 8 bit numbers through 2 LVDS pads. In strip mode, the chip

#### DECAL

multiplexes across all columns, sending out 2 bits for each, representing 0, 1, 2, or many hits. This mode requires all 4 LVDS pads for data transmission.



Figure 3 Asynchronous column summation

Figure 4 Peripherial logic arrangements

#### 4. Test Results

The chip has been fabricated on 18um high resistivity epitaxial silicon in a 180nm CMOS process. In the following sections, we report the results of simulated and measured noise as well as digital test, other analogue pixel output response have already been published elsewhere [3] [4].

#### 4.1 Analogue testing

The first tests of analogue response of the pixel were already reported on [3] [4]. Preamplifier and output of the pixels are in accordance with simulated data of the same nodes.

The noise was then measured by scanning the threshold while constantly illuminating the pixel externally with a laser to imitate a particle detection. The range of the threshold voltage which results in hits is histogrammed and the standard deviation of this histogram represents the measured noise of the pixel. Figure 5 shows the transient noise simulations (left) compared to the measured noise based on the threshold scan (right)

The results give a noise of 3mV, which is in good agreement with the simulation result of 5mV. Evaluating this noise in electrons would require measurement of the conversion gain using Fe55 or similar, which has yet to be performed. The simulated conversion gain is 36uV/e-. If this is accurate, then the input referred noise would be 83e-



Figure 5 Histograms for transient noise simulations of the pixel (left) and noise test results of the manufactured pixel (right) [4].

#### 4.2 Digital testing

The chip was first tested in strip mode by clocking data into the test register and reading out the result from the LVDS channels. A single "11" pattern was loaded into the register and clocked across the array. In strip mode, since each column can output two bits, the total output of the chip is a 128 bit stream. Therefore, if the chip is operating correctly, as the 2 bit pattern moves into the test register for each strip in turn, the next two bits in the output stream should set to 1. This is indeed what is observed, as shown in Figure 6.

The chip was then tested in pad mode. In this case, 2 tests were performed. In the first, the 5 bit pattern b'01111 was clocked continuously into the test register. In this case, once the 16 columns attached to a single summing output have received the pattern, the output total should reach 240. Continuing to clock the pattern in will lead to all summed outputs reaching 240.

In the second test, the clocked in pattern is b'10000. This sets the overflow bit of every strip. Therefore, in this case the summed output stays zero, and the overflow sum increases until it reaches 16. This then continues across all outputs. Figure 7 shows this occurring as expected.



#### 5. CONCLUSION

In this paper, we have described a re-configurable monolithic active pixel sensor for calorimetry and tracking. The operation of the sensor was described, and test results presented for the analogue and digital sections.

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