PROCEEDINGS OF SCIENCE

ALTIROC1, a 25 pico-second time resolution ASIC for the ATLAS High Granularity Timing Detector (HGTD)

Nathalie Seguin-Moreau[1]
OMEGA/CNRS/Ecole Polytechnique
91128 PALAISEAU CEDEX, France
E-mail: nsmoreau@in2p3.fr

Other Authors

S. Conforti, P. Dinaucourt, C. de La Taille, G. Martin-Chassard
OMEGA/CNRS/Ecole Polytechnique
E-mail: taille@in2p3.fr

C. Agapopoulou, N. Makovec, L. Serin, S. Sacerdoti
LAL/CNRS/Université Paris Sud
91405 ORSAY CEDEX, France
E-mail: sabrina.sacerdoti@cern.ch

A. Dragone, B. Markovic, C. Milke, L. Ruckman, A. Schwartzman, D. Su
SLAC National Accelerator Laboratory
94025 MENLO PARK California, United States of America
E-mail: markovic@slac.stanford.edu

D. Gong, J. Ye, W. Zhou
Southern Methodist University
Dallas, TX 7527594025, United States of America
E-mail: dgong@mail.smu.edu

ALTIROC1 is a 25-channel ASIC designed to read out the 5 x 5 matrix of 1.3 mm x 1.3 mm x 50 µm Low Gain Avalanche Diodes (LGAD) of the ATLAS HGTD detector foreseen for the HL-LHC upgrade. The targeted combined time resolution of the sensor and the readout electronics is from 40 ps/hit (initial) to about 80 ps/hit (end of operational lifetime). Each ASIC channel integrates a RF preamplifier followed by a high speed discriminator and two TDCs for Time-of-Arrival and Time-Over-Threshold measurements as well as a local memory. This front-end must exhibit an extremely low jitter noise while keeping a challenging power consumption of less than 4.5 mW. Detailed measurements are presented.

TWEPP 2019
2-6 September 2019
Santiago de Compostela

[1]Speaker

PoS(TWEPP2019)042

1. Introduction

The expected increase of the particle flux at the high luminosity phase of the LHC (HL-LHC) will have a severe impact on the object reconstruction (jets, electrons, b tagging) performance in the forward region due to the large number of pile-up interactions. A High Granularity Timing Detector is proposed in front of the Liquid Argon end-cap calorimeters for pile-up mitigation and for bunch per bunch luminosity measurements. This detector will cover the pseudo-rapidity range of 2.4 to about 4.0 and will be equipped with two double sided layers of Low Gain Avalanche Detectors (LGAD) with 1.3 x 1.3 mm^2 pads. It will be made of two independent rings, with a coverage from a 120 mm (resp. 320 mm) to 320 mm (resp. 640 mm) radius. The aim is to provide a timing information for minimum ionizing particle with a precision between 30-50 ps over the detector's lifetime. ALTIROC1 is a 25-channel ASIC prototype designed to read out the 5 x 5 matrix of 1.3 mm x 1.3 mm x 50 µm Low Gain Avalanche Diodes (LGAD). Each channel integrates a high speed preamplifier followed by a discriminator, two TDCs, one for Time of Arrival (TOA) and one for Time-Over-Threshold (TOT) measurements and a SRAM to store digitized data.

2. ALTIROC1 architecture

2.1 ASIC requirements

The requirements are summarized in Table 1. Each channel will read out data coming from 1.3 x 1.3 mm^2, 50 µm active thickness sensor pads, corresponding to a detector capacitance of around 4 pF. The targeted time resolution is 30 ps rms per track combining multiple hits and 50 ps rms after 4000 fb^{-1}. The time resolution per hit must therefore be smaller than about 40 ps at start and smaller than 85 ps (70 ps) for the inner ring (outer ring) at the end of the lifetime. To achieve such a performance, the electronics jitter for an input charge of 10 fC (equivalent to the charge deposited by a MIP in a 50 µm thick LGAD with a gain of 20) is required to be of the order of the dispersion induced by the Landau fluctuations in the energy deposit, which limits the time resolution to 25 ps. As for the time walk contribution, it must be corrected with an accuracy leading to a residual contribution better than 10 ps rms for signals ranging from 1 MIP to 10 MIPs, which corresponds to 10 to 100 fC (with a LGAD gain of 20).

PAD size	1.3 x 1.3 mm^2 => **Cdet = 4 pF**
ASIC size and channels/ASIC	2 x 2 cm^2 225 channels/ASIC
Single PAD noise (ENC)	**< 1500 e- or 0.25 fC**
Minimum threshold	**1 fC**
Dynamic range	**2.5 fC** to 100 fC
Maximum jitter (σ_{elec})	**25 ps at 10 fC at the start of the HL-LHC and 70 to 85 ps after 4000 fb-1 for 2.5 fC**
TDC contribution	**< 10 ps**
Time walk contribution	**< 10 ps**
TDC conversion time	**< 25 ns**

Table 1: ALTIROC final ASIC requirements

The ASIC is designed in CMOS 130 nm. At low radius, the expected TID and fluence are respectively 9.5 MGy (including a safety factor of 2.25) and 10^{16} n/cm^2 (including a safety factor of 1.5). The radiation levels in the forward region will then exceed the radiation hardness of both sensors and electronics, especially at low radius. The current strategy is therefore to replace the inner ring of each layer after 2000 fb^{-1}. As the sensor charge will decrease under irradiation, the

discriminator threshold should be set to small enough values to detect input charges as low as 2.5 fC (resulting in a jitter larger than 25 ps).

The power dissipation of a complete pixel readout must be limited to 4.4 mW, split in 2.2 mW for the analog part including the Time to Digital Convertors (TDC) and 2.2 mW for the pixel digital processing to cope with the expected power of the CO2 cooling system used in ATLAS.

2.2 Single channel architecture

2.2.1 Preamplifier and discriminator

The input stage consists of a high speed (~1 GHz) voltage preamplifier, followed by a large gain leading edge discriminator, both of which are critical elements for the overall electronics time measurement. They are described in details in [1]. The discriminator rising edge provides the Time-Of-Arrival measurement (TOA) and its width the Time-Over-Threshold (TOT) measurement for time walk correction.

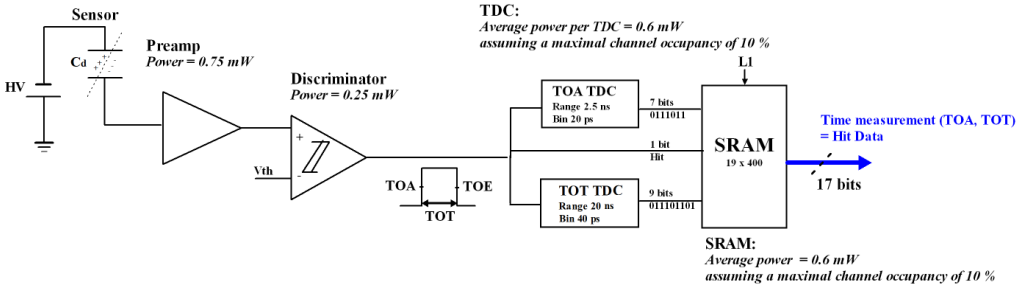

Figure 1: ALTIROC readout channel with power consumption of each block

2.2.2 TOA and TOT Time-to-Digital Converters and local memory

Two Time-to-Digital converters (TDC) perform the digitization of the TOA and TOT information provided by the discriminator output. Details can be found in [2]. The TOA TDC provides a 7-bit digitization on a 2.5 ns range with a 20 ps bin. As this quantization step is below the gate-propagation delay in 130 nm technology, a Vernier line configuration is employed. It consists of two lines, a fast and a slow one, each made of delay cells (Figure 2).

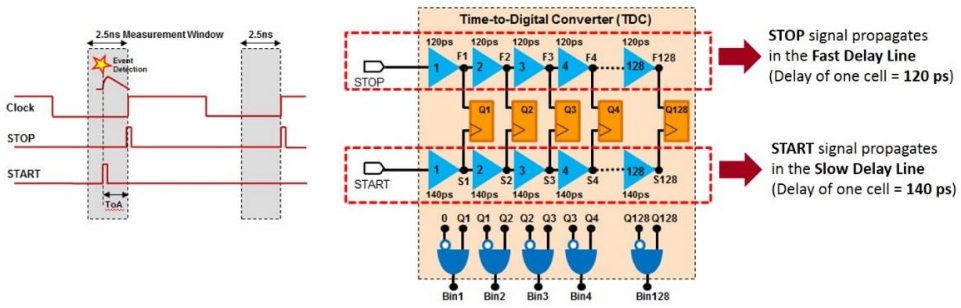

Figure 2: Simplified schematic of the TOA TDC

A control voltage provided by a DLL sets the delay of the slow line delay cells to 140 ps and to 120 ps for the fast line delay cells. The TOA is measured within a 2.5 ns window centered at

the bunch-crossing. The START signal (rising edge of the discriminator) enters the slow line while the STOP signal (rising edge of the 40 MHz clock) enters the fast delay line. The number of cell stages necessary for the STOP signal to surpass the START signal gives the time measurement with a bin of 20 ps. Since the time measurement is initiated only upon signal detection, the reverse START-STOP scheme is used as a power saving strategy.

The TOT TDC provides a 9-bit digitization of the discriminator width, on a 20 ns range. It uses an additional coarse delay line made of 160 ps delay cells to extend the measurement range to 20 ns, while a Vernier delay line provides the requested fine resolution of 40 ps. The START and STOP signals are given by the rising edge and by the falling edge of the discriminator respectively.

A circular SRAM is integrated to store the 16 bits of the time measurement as well as the hit bit until a L0/L1 trigger [2]. To save power, data are stored only in case a hit occurs.

2.3 Measurements

2.3.1 Prototypes

A first prototype, Altiroc0, with 4 channels was designed and tested in 2017 and 2018 [1] in order to evaluate the very font-end performance (preamplifier and discriminator). Then, in 2018, Altiroc1 was designed with 5 x 5 complete channels to read out 5 x 5 sensor matrix of 1.3 x 1.3 mm^2 LGAD sensors. These ASIC were tested on testbench, under TID irradiation and recently in testbeam conditions. The test setup consists of an ASIC board connected through a cable to a custom FPGA board. On channel 4 of each column, a capacitor can be connected through a programmable switch to the preamplifier input to mimic the LGAD sensor capacitance and thus to study the performance as a function of the detector capacitance. This capacitance is tunable from 0 to 7 pF with a 1 pF step. In addition, an internal pulser is integrated to calibrate each channel. It generates a programmable voltage step (Vstep) at the input of each pixel through an internal Ctest capacitor of 200 fF selectable by slow control. A known input charge equal to Ctest*Vstep can therefore be injected in each channel.

2.3.2 TOA and TOT TDC measurements

The characterization of the TOA TDC was achieved by delaying the input pulse with a 10 ps delay. The measured quantization step (LSB) of the TOA TDC was found to be around 20 ps and the range around 2.5 ns as expected (Figure 3, left).

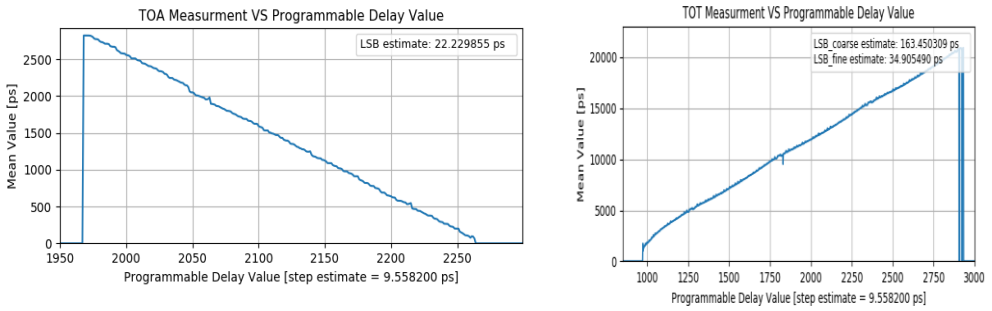

Figure 3: TOA versus delay of the input signal (Left). TOT vs width of external trigger (Right)

The TOA LSB measured on 15 channels before calibration varies from 17 ps to 21 ps. Similarly, the range of the TOT TDC was measured and can reach 20 ns. The coarse TOT LSB

and the fine TOT LSB are respectively around 160 ps and around 40 ps as expected (Figure 3, right). Each pixel TOA and TOT LSB can be fine-tuned using slow control parameters.

Figure 4 shows the measurement of the TOA jitter variation of two channels as a function of the injected charge for a detector capacitor of 4 pF set by slow control.

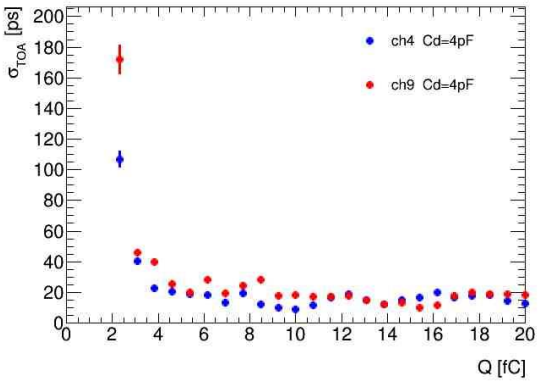

Figure 4: TOA Jitter vs injected charge with Cd=4 pF

The threshold can be set to values smaller than 2 fC and a jitter smaller than 25 ps (resp. 40 ps) was measured on both channels for an injected charge of 10 fC (resp. 4 fC). The 10 ps floor is attributed to the TDC LSB and the command pulse jitter.

Two tree distributions, one for the 40 MHz clock and one for the command pulse used for the internal pulser are integrated. The measured TOA LSB dispersion between channels is 18 ps ± 4 ps before any adjustment. Although such contribution is not a dominant term in the time resolution, it could be further reduced by tuning individually each TOA LSB through the slow control parameters.

2.3.3 Irradiation tests

Altiroc1 was irradiated at CERN with Xrays up to 340 Mrad. Tests were focused on the preamplifier and the discriminator. A small decrease of the preamplifier amplitude was observed as well as a small increase of the discriminator jitter (Figure 5).

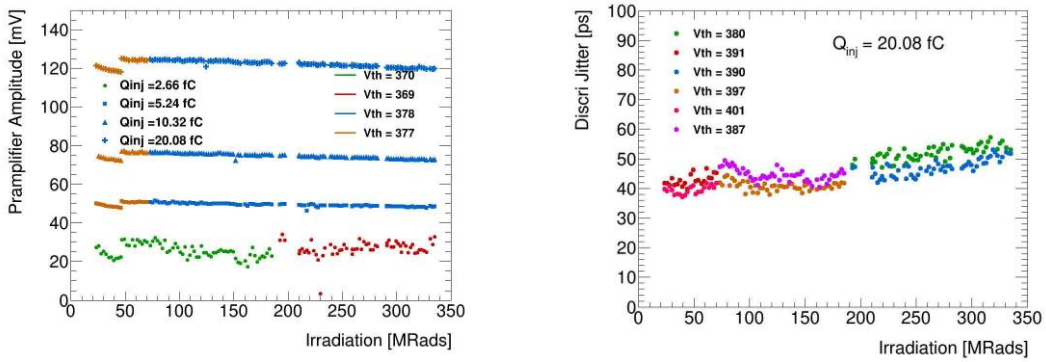

Figure 5: Preamplifier amplitude (Left) and discriminator jitter during irradiation (Right)

DC voltages such as the bandgap output, the 10-bit DAC used to set a common discriminator threshold as well as the 7-bit DAC used for individual tuning of the threshold were also followed during the irradiation and showed variations smaller than 20 mV (around 800 mV) between 20 Mrad and 340 Mrad.

3. Conclusion

Test bench measurements of ALTIROC1 show good results, in particular an electronics jitter better than 25 ps for a detector capacitance of 4 pF and an injected charge of 10 fC. Test beam measurements performed in August 2019 with LGAD sensor bump bonded onto the ASIC are under analysis. The final version of the ASIC, ALTIROC2, with 225 channels, is under design and will be submitted in Spring 2020.

Acknowledgements: We acknowledge IFAE (Barcelona), CNM (Barcelona) and IHEP (Beijing) for flip-chip assembly and LPC (Clermont) for board assembly

References

[1] C. de La Taille et al, *Altiroc0, a 20 ps time resolution ASIC for the ATLAS HGTD*, TWEPP17 proceedings, *PoS TWEPP-17 (2018) 006* **01** (3021) 006

[2] B. Markovic et al, *Altiroc1, a 20 ps time resolution ASIC prototype for the ATLAS HGTD*, IEEE 2018 proceedings, DOI: 10.1109/NSSMIC.2018.8824723.