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Development of RD50-MPW2: a high-speed monolithic HV-CMOS prototype chip within the CERN-RD50 collaboration

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The CERN-RD50 collaboration has ongoing research to further develop monolithic High Voltage-CMOS (HV-CMOS) sensors in a 150 nm process for future particle physics experiments. As a part of this research programme, a test chip (RD50-MPW2) that implements new methodologies for low leakage current and fast and low-noise readout circuitry has been designed and submitted for fabrication. This article presents the design details and simulation results of the 8 × 8 matrix of high-speed monolithic HV-CMOS pixels included in RD50-MPW2, in which two flavours of fast pixels are implemented: a conventional continuous-reset pixel and a switched-reset pixel with a novel asynchronous switched-reset scheme.

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1. Introduction

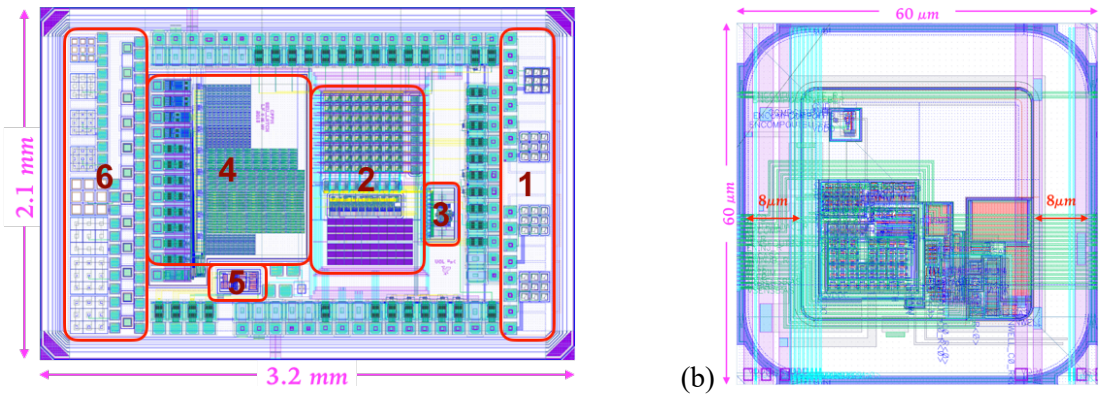
Because of their excellent radiation tolerance to high integrated fluences (2×10^{16} 1 MeV n_{eq}/cm^2), precise time resolution (~ 1 ns) and capability to cope with high hit rates (~ 3 GHz/cm^2), hybrid pixel detectors are widely used in current particle physics experiments [1]. However, due to their multi-layer nature, hybrid detectors have substantial thickness (300 µm), which limits their accuracy in particle tracking. In addition, the bump-bonding process to assemble the sensor and the readout chip is expensive (~ 1 M£/m^2), time-consuming and restricts pixels to minimum sizes of 55 µm × 55 µm, making it challenging to achieve fine granularity.

Alternatives to the hybrid detectors are the monolithic sensors in commercial CMOS processes [2]. Since the sensing diode and the readout electronics are integrated into a single layer of silicon, CMOS sensors avoid the complex hybridization process. The one-layer structure allows thinning the detectors down to 50 µm. However, their slow charge collection by diffusion and low radiation tolerance (10^{13} 1 MeV n_{eq}/cm^2) [3] limit the application of CMOS sensors to low rate and low radiation experiments only, such as the ALICE Inner Tracker System (ITS) Upgrade. To achieve monolithic sensors with advanced performance, High Voltage CMOS (HV-CMOS) sensors [4] are being developed for faster charge collection by drift and higher radiation tolerance (10^{15} 1 MeV n_{eq}/cm^2) [5]. The Mu3e experiment at the Paul Scherrer Institute (PSI) in Switzerland has adopted monolithic HV-CMOS sensors for its pixel tracker [6] and other experiments, such as the LHCb Upgrade Ib and II and CLIC, are considering this sensor technology as well.

This article describes ongoing research within the CERN-RD50 collaboration to further develop monolithic HV-CMOS sensors in a 150 nm process for future particle physics experiments. In particular, it focuses on the design work of RD50-MPW2, the second prototype developed by the collaboration, aimed at minimizing the leakage current of the sensor and developing fast and low-noise readout circuitry.

2. RD50-MPW2

The layout of RD50-MPW2 is shown in figure 1(a). The chip is produced on 10 Ω·cm, 200 - 500 Ω·cm, 1.9 kΩ·cm, and 3 kΩ·cm substrate resistivity wafers. This prototype includes test structures (marked as 1 and 6 in the figure), an 8 × 8 pixel matrix (2), an analog buffer (3), a Single Event Upset (SEU) tolerant memory array (4) and a bandgap voltage reference (5). Compared with the previous version RD50-MPW1, this chip reduces the leakage current by preventing certain filling layers added by the foundry and adding a series of guard rings [7].



(a) (b)

Figure 1. (a) Layout of RD50-MPW2 and (b) layout of one pixel.

2.1 Pixel matrix

This article focuses on the design of the 8 × 8 pixel matrix, in which two flavours of fast readout circuits are implemented to verify the functionality of HV-CMOS pixels with new methodologies for low leakage current, high response rate and fine time resolution. The pixel size is 60 µm × 60 µm as shown in the pixel layout in figure 1(b). Each pixel flavour consists of a high impedance circuit to bias the collecting electrode, a Charge Sensitive Amplifier (CSA) based on a single-ended folded cascode amplifier with PMOS input as shown in figure 2(a), a source follower, a high-pass filter and a CMOS comparator with a local 4-bit Digital to Analog Convertor (DAC) for threshold tuning. As observed, the area in the upper half of the pixel layout is empty and will be occupied by digital readout circuits in a future version of the design. Analog signals generated by the pixels at the output of the CSA and the comparator can be measured either via the analog buffer or directly through output pads.

2.2 High response rate

To cope with the high hit rate foreseen in future experiments (2 - 4 GHz/cm^2 for High Luminosity-LHC), it is necessary to improve the response rate to avoid pile-ups in single pixels. A high response rate can be achieved with an amplifier that has short rising and falling edges when in response to a particle hit.

The rising edge duration is given by $t_{rise} \propto C_d / g_m$, where C_d is the detector capacitance and g_m the transconductance of the CSA input transistor (M0 in figure 2(a)). C_d is mainly the capacitance between the P-substrate and the deep n-well ($C_{sub/DN}$ in figure 2(b)) and that between the deep p-well (PSUB) and the deep n-well ($C_{PSUB/DN}$). With a given pixel size and p-well/deep n-well spacing, the deep n-well area and therefore $C_{sub/DN}$ are fixed. $C_{PSUB/DN}$ can be minimised by reducing the size of the PSUB layer which isolates the n-well from the deep n-well layer and thus allows full CMOS logic in the sensing area of the pixel. The values of $C_{sub/DN}$ and $C_{PSUB/DN}$, simulated with Cadence at -60 V of sensor biasing, are 80 fF and 70 fF respectively. g_m is increased by optimizing the geometry and the drain current of M0. With a low C_d and a large g_m, the rising edge duration is decreased.

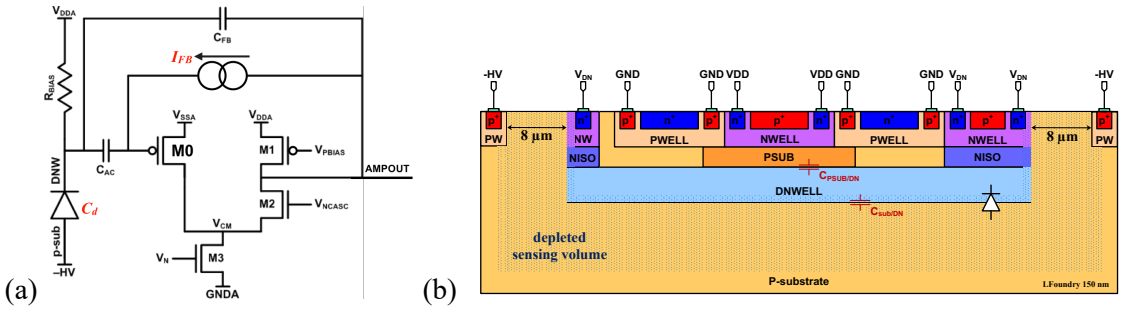


Figure 2. (a) Schematic of the CSA and (b) Cross-section of the pixel

The falling edge duration is given by $t_{fall} \propto 1 / I_{FB}$, where I_{FB} is the feedback current that resets the pixel after each event. Two pixel flavours with different methods to reset the pixel are implemented in this work. One flavour is the continuous-reset pixel, which is shown in figure 3(a). In this conventional pixel flavour, its feedback current I_{FB_CONT} is constant. The input charge Q accumulated over the feedback capacitance is linearly discharged and the fall time can be written as $t_{fall} = Q / I_{FB\_CONT}$. Thus, the time to reset the CSA is proportional to the input charge and the Time over Threshold (ToT) can be measured. Although a large I_{FB_CONT} decreases t_{fall}, it

also lowers the charge-to-voltage gain and increases the noise. Therefore, the falling edge duration can only be shortened to a limited extent in this pixel flavour.

The other flavour is the switched-reset pixel, shown in figure 3(b), where a switched large current I_{FB_SW} discharges Q in less than 5 ns. Switched-reset pixels have been explored in previous works, where a clock signal controls the switch for a synchronous periodic reset [8]. However, that option limits the reset frequency (1 MHz in [8]) and induces crosstalk noise by clock feedthrough. In this work, the switch is asynchronously controlled by the in-pixel comparator. The mechanism is as follows: 1) The output of the comparator COMPOUT toggles to high when a charged particle hits the pixel. 2) After a delay of 15 ns, the switch is closed and I_{FB_SW} starts discharging C_{FB} and resets the CSA in less than 5 ns. 3) COMPOUT returns to its low level and opens the switch again. Because I_{FB_SW} flows only in the reset phase, its value can be rather high without affecting the charge sensitivity and the noise. The Time of Arrival (ToA) can be achieved. This pixel flavour is suitable for experiments that require binary information.

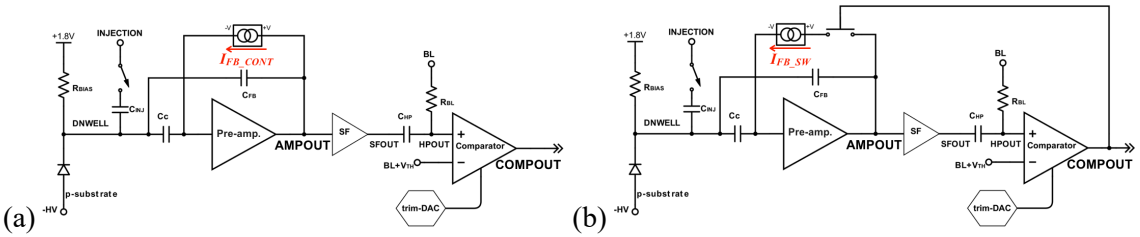


Figure 3. Schematics of (a) the continuous-reset pixel and (b) the switched-reset pixel

2.3 Fine time resolution

The time resolution reflects the accuracy of the ToA measurement. The ToA is recorded when the amplified signal of a particle hit surpasses the threshold voltage V_{TH}. The measured ToA depends on the charge collection time of the sensor and the response time of the front-end electronics. The uncertainties associated to these two factors cause the amplified signals of particles that generate different amounts of charges in the sensor to cross V_{TH} with different time delays. This time difference is called time-walk and limits the time resolution.

The response time of state-of-the-art HV-CMOS sensors dominates the time-walk. Assuming the rising edges of amplified signals of two particles have slew rates of $SR - \Delta SR$ and $SR + \Delta SR$, and the time they need to reach V_{TH} is $\frac{V_{TH}}{SR-\Delta SR}$ and $\frac{V_{TH}}{SR+\Delta SR}$, the time difference is $\frac{V_{TH}}{SR-\Delta SR} - \frac{V_{TH}}{SR+\Delta SR} = V_{TH}\frac{2\Delta SR}{SR^2-\Delta SR^2} \approx V_{TH}\frac{2\Delta SR}{SR^2}$. This expression shows that the time-walk can be reduced by decreasing V_{TH} and increasing SR. With the threshold voltage constrained by the noise of the sensor, the slew rate is increased by shortening the rising edge of the CSA in this work. As a result, the time resolution is improved.

2.4 Simulation results

Post-layout simulation results in figure 4 show the response of the continuous-reset and switched-reset pixels to input charges ranging from 1 ke^- to 10 ke^- when I_{FB_CONT} and I_{FB_SW} are set to 15 nA and 1 µA. Table 1 summarizes and compares performance of both pixel flavours together with that of the pixel in RD50-MPW1, when the input charge is 5 ke^-. The response time is the time the output of a hit pixel takes to recover its baseline voltage.

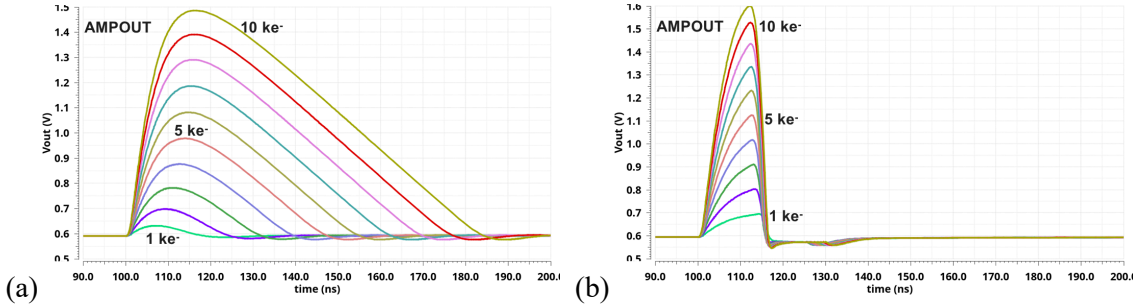


Figure 4. Simulation results of (a) the continuous-reset pixel and (b) the switched-reset pixel

Input: 5 ke⁻	pixel size	gain	response time	ENC	time-walk	power cons.
Continuous-reset pixel	60 μm × 60 μm	50 μV/e⁻	53 ns	120 e⁻	7.8 ns	24 μW/pixel
Switched-reset pixel	60 μm × 60 μm	80 μV/e⁻	32 ns	100 e⁻	6.4 ns	25 μW/pixel
RD50-MPW1 pixel	50 μm × 50 μm	30 μV/e⁻	125 ns	115 e⁻	11 ns	23 μW/pixel

Table 1. Pixel performances of RD50-MPW2 and RD50-MPW1

3. Conclusion

The RD50-MPW2 prototype developed in the CERN-RD50 collaboration is designed to have low leakage current and fast readout circuitry. An 8 × 8 pixel matrix with two pixel flavours for high response rate and fine time resolution has been implemented in this chip. A novel asynchronous switched-reset front-end is proposed. Post-layout simulations of the two pixel flavours show their good performance in terms of response time (30 ns and 50 ns for a 5 ke⁻ signal), time walk (~ 8 ns) and noise (ENC ~ 100 e⁻).

Acknowledgement

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