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LAUROC1 : Liquid Argon Upgrade Read Out Chip

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The analog front-end readout electronics of the ATLAS Liquid Argon (LAr) Calorimeter will be replaced by a single chip for the phase II of the high luminosity Large Hadron Collider at CERN. The cornerstone of the circuit is the preamplifier which is very demanding in terms of low noise (0.4 nV/√Hz), large dynamic range (up to 10 mA, 16 bits) and precise input impedance (25 or 50 Ohms) to terminate the cables from the detector. LAUROC1 ASIC integrates an innovative architecture to fulfil these requirements.
Detailed measurements are presented.

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1. Introduction

The increase of the luminosity at the LHC implies higher energy events and so necessitates an upgrade of the current ATLAS Liquid Argon Electromagnetic Calorimeter readout electronics to fulfil a larger dynamic range. Another goal of this upgrade is to speed up the digitization up to 40 MHz and to provide fully digitized data to the trigger.

LAUROC1 ASIC is designed in CMOS 130 nm and integrates four analog front-end channels. Each channel consists of a preamplifier followed by a High-Gain (HG) and a Low-Gain (LG) CRRC2 differential shaper. The two-gain shaper accommodates the large dynamic range of the LAr signals to the external 14-bit ADC. Their bipolar waveform optimizes the signal to noise ratio in the presence of the anticipated pileup and acts as anti-aliasing for the following 40 MHz ADC.

The cornerstone of the analog Front-End is the preamplifier, which is current sensitive due to the long signal duration (450 ns) of the liquid argon pulse. The input impedance has to be precisely matched to the cable impedance bringing the signals out of the cryostat (25 and 50 Ω). As always in calorimetry, the dynamic range is very large, with detector current reaching up to 10 mA and the detector capacitance ranges from 400 pF to 2.2 nF. The dynamic range is split in two 14 bits ranges, with a gain ratio of 16 and a linearity at per-mil level on both ranges. The most stringent requirement is actually the very low noise, where an Equivalent Noise Current (ENI) must be smaller than 200 nA for a detector capacitance of 1.5 nF. This corresponds to a noise spectral density of 0.4 nV/√Hz, equivalent to a 10 Ω resistor, hence the denomination of "electronically cooled resistor".

2. LAUROC1 architecture

2.1 Preamplifier

The schematic diagram of the preamplifier is shown in Figure 1 and described in [1].

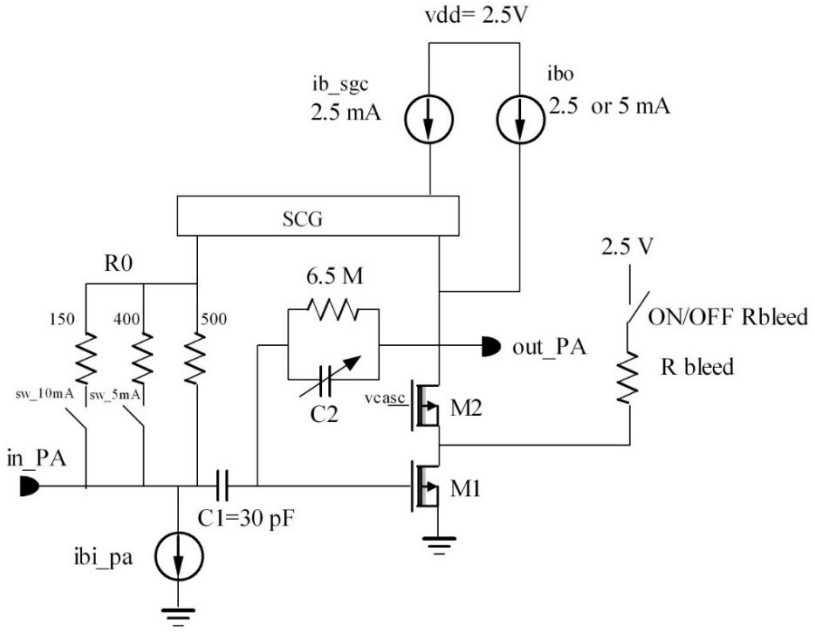

Figure 1: schematic diagram of the preamplifier. The SCG block is a low impedance current converyor ("super common gate") All bias currents are internal. The switches are activated by slow control.

The preamplifier is built around an amplifier with two feedback paths R0 and C2. The variable feedback capacitor C2 allows to tune the input impedance as Rin = R0 C2/C1. The feedback resistor R0 can be adjusted in order to optimize the preamplifier dynamic range : R0 = 1 kΩ is used for the calorimeter front section, whereas R0 = 100 Ω for the middle and back sections which receive input currents up to 10 mA.

The noise is dominated by the series noise of M1, which amounts to 0.3 nV/√Hz with a 5 mA drain current and by the thermal noise of the feedback resistor R0 divided by the preamp gain C2/C1 to the square. The detailed calculation and simulations are given in Ref [1].

2.2 Single channel architecture

The schematic diagram is shown in Figure 2. The high gain is obtained by cascading two input preamplifiers in order to minimize the second stage noise. The shaper was designed by the Brookhaven team on a CRRC² architecture, with a variable peaking time in order to compensate for process variations. The full ASIC incorporates 4 channels in order to characterize the crosstalk and the coherent noise. Three channels are identical and the fourth channel is a legacy channel from the previous prototype LAUROC0 [1].

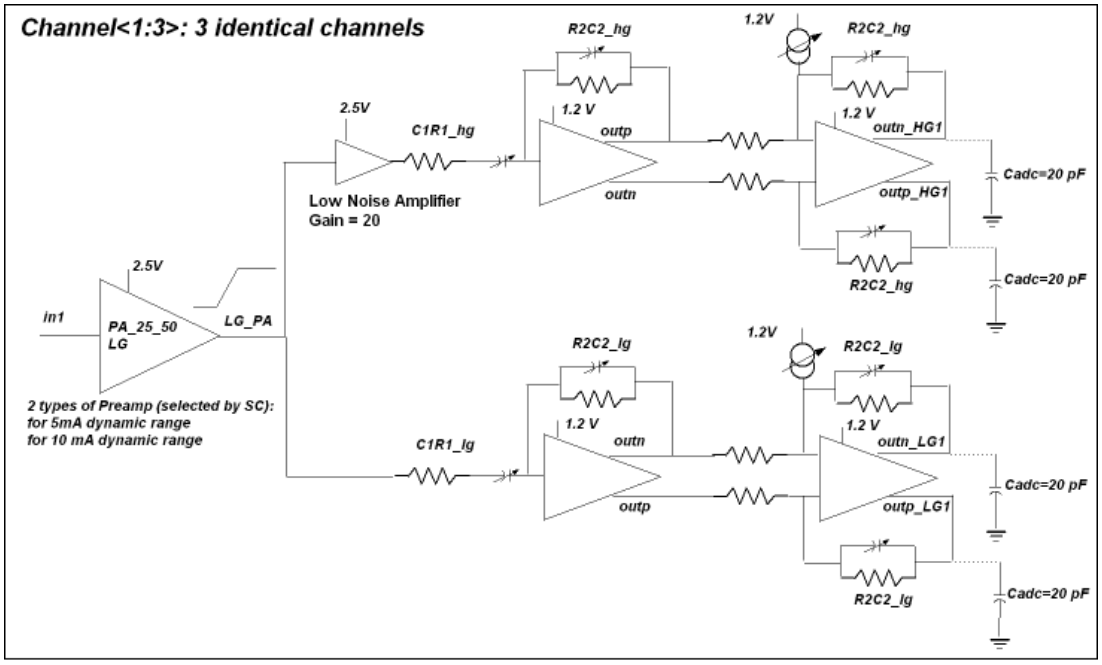

Figure 2: single channel architecture

The ASIC is designed in CMOS 130 nm. The radiation levels are expeted below 2.5 kGy, which is small for this technology which was tested up to several MGy. The power dissipation is not critical in this detector and amounts to 100 mW/channel.

3. Measurements results

The measurements presented here concentrate on the noise performance, where some discrepancies were found with respect to the simulation.

3.1 Signal measurements

The signal measurements correspond very well to the simulations. The input impedance can be tuned to 25 Ω or 50 Ω with a ±10% range and an accuracy of 0.5 Ω. The shaping time is also in good agreement with simulations with a tuning range of ±25% around the nominal 15 ns time constant. Apart from the noise, the most important parameter for the calorimeter is the linearity, which needs to be at the per-mil level up to 9 mA input current, which is achieved as shown in Figure 3.

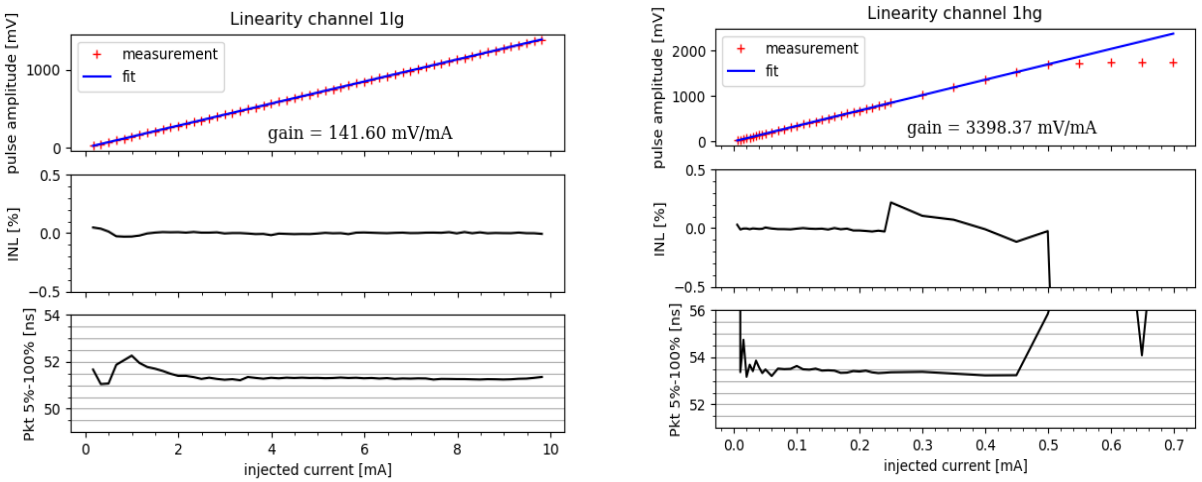

Figure 3: Integral non-linearity on High gain and Low gain shaper outputs.

3.2 Noise measurements

A first series of noise measurements were carried out on the input transistor alone on the previous prototype LAUROC0, as the preamplifier noise was much larger than expected. They are recapitulated in Figure 4. It can be seen that the simulation models were overly optimistic (by almost a factor 2 at 1 mA drain current) compared to the theoretical expectation of 2kT/gm in weak inversion. This was due to improper simulation models in the design kit for large transistors which we could not change, despite several requests. We resimulated with older models, which did not take into account weak inversion, modelizing the series noise as 8kT/3gm. Although slightly pessimistic, the simulations were at least not better than theory and allowed to check the various additional noise contributors to verify that the input transistor was well dominating.

It can also be seen and that the noise was 50% too large at the nominal 5 mA drain current, which explained the poor noise performance. The extra noise was due due to the resistance of the deep n-well injected through the back gate. The layout was changed to minimize this extra noise source by adding multiple contacts. It was remeasured separately, as shown in Figure 4, and the new input transistor noise is now very close to the theroretical expression. This new layout was then used in LAUROC1.

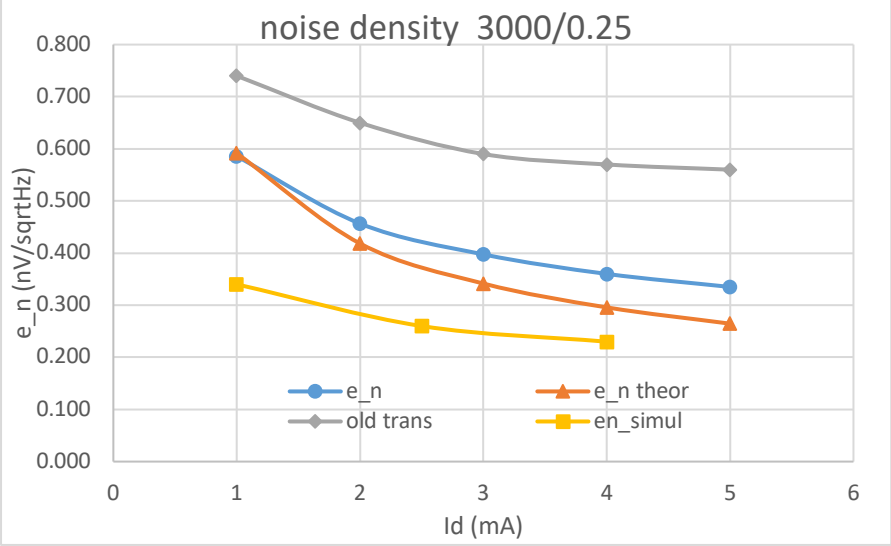

Figure 4:measured Noise spectral density of the input transistor. The yellow and orange curves correspond respectively to simulation and theory (2kT/gm). The grey and blue correspond to the measurements of a previous layout and of the final layout with optimized deep nwell.

The noise measurements of the full chip still exhibit a noise larger than simulated by 20%. To understand the discrepancy, the preamplifier was measured without the R0 feedback path, as if it were a charge sensitive preamplifier with a detector capacitance equal to C1=30 pF. The gain was maximized by setting C2 = 1 pF and a low noise external shaper was used to vary the shaping time. This allowed to extract the series, parallel and 1/f noise components. LAUROC shaping corresponds to tp = 30 ns and it can be seen that the noise is 20% higher due to the 1/f noise. It is also interesting to see that the series noise corresponds well to the series noise extracted from simulations, with Cd = 36 pF and en = 0.45 nV/√Hz. The extra 6 pF in addition to C1 correspond to the input transistor, C2 and parasitics. The extra series noise corresponds to the additional noise sources (cascode, current sources as the input transistor contributes to 70% of the total noise).The current was also varied in the input transistor, leading to lower series noise but unchanged 1/f noise. As the input transistor and current sources were measured separately with much lower 1/f noise, the only remaining contribution is the MIM capacitors used to form C1 and C2. A dielectric loss of tan δ = 0.002 for SiO_2 would give an ENC of 280 e- rms, compatbile with the value of 320 e- obtained by the fit. It is unfortunately not feasible to move C1 outside of the chip to remove its dielectric noise as the additional parasitic capacitance on the preamplifier input would increase the series noise by an amount similar to the decrease of 1/f noise.

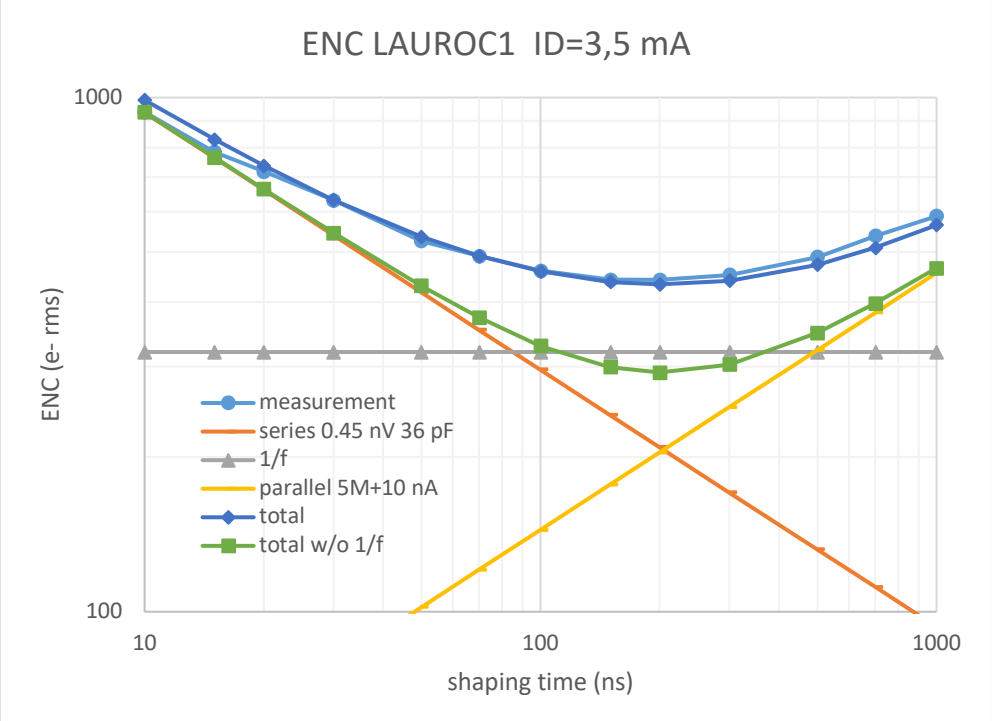

Figure 5: equivalent noise charge of the preamplifier alone with external variable shaper. The ENC fit shows the series and parallel noise as expected but an extra 1/f component responsible for the 20% noise increase at tp=30 ns corresponding to ATALS shaping.

4. Conclusion

Test bench measurements of LAUROC1 show good results for input impedance and linearity over the full range. The noise is larger than simulations by 20%, attributed to the dielectric losses in the MIM capacitors. The final version of the ASIC, LAUROC2 was submitted in september 2019.

References

[1] F. Dulucq *et al*., "LAUROC: “A new electronically cooled line-terminating preamplifier for the ATLAS liquid argon calorimeter upgrade”," *2016 IEEE Nuclear Science Symposium, Medical Imaging Conference and Room-Temperature Semiconductor Detector Workshop (NSS/MIC/RTSD)*, Strasbourg, 2016, pp. 1-5.
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