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A Precision Pure Clock Distribution System

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Both the ATLAS and CMS Collaborations are planning to install new detectors designed to measure the time of arrival of particles produced at the CERN LHC to a precision of 30 ps or better. An essential component of any of these detectors is the reference clock that has to be distributed to multiple sites across the detector, aligned to better than 10 ps. This report describes a clock distribution system suitable for these large scale applications and the demonstration of the achievement of an inter-clock stability of less than 1 ps.

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1. Introduction

When the CERN High-Luminosity LHC reaches its design luminosity the number of collisions per bunch crossing at the interaction points of the ATLAS and CMS detectors will exceed 140. This high 'pile up' of events poses a significant challenge in the analysis of data that will be collected there. To mitigate this problem both collaborations are planning on installing detectors capable of measuring the time of arrival of hadronic and electromagnetic particles with a precision of 30 ps or less. With these detectors the vertex of an event of interest can be selected by effectively dividing the duration of the beam overlap, which is ≈350ps, into narrow time slices, effectively reducing the level of background events to ≤ 40, the level of pile-up currently experienced at the LHC.

For the upgrade of the CMS detector there will be two sub-detectors built expressly for this purpose with resolutions of 30 ps, and, in addition, the front-end electronics of the electromagnetic calorimeter will be upgraded to measure the time-of-arrival of electromagnetic showers to a similar precision. One of the central problems in designing these detectors is the distribution of a clock signal to all of the detector components with a precision significantly better than the timing measurement requirement of 30 ps. In all, close to half-a-million channels will need to be instrumented with precision reference clocks. All of these precision clocks will be derived from the LHC clock and distributed with clock frequencies of 40, or 160, or 320 MHz to the detector systems.

One approach is to use the CERN-designed low-power gigabit transceiver (LpGBT). In this approach a 2.56 Gbs clock and control signal, aligned with the LHC clock, is sent from the off-detector electronics to the on-detector readout. There the clock signal is recovered using a clock data recovery circuit that is integrated into the LpGBT. While this approach minimizes the number of fibers required to distribute the clock, it has the drawback of being a complex system that will be simultaneously used for 10 Gbs data transmission in a high radiation environment. As an alternative approach to the problem of clock distribution, we are investigating the use of modern discrete radio-frequency quality components to distribute an unencoded or 'pure' clock.

In this report we describe the design of this system and the performance achieved so far.

2. System Design

To test and demonstrate the possibility of distributing a precision clock directly to the detectors, we have built a system that can be configured differently to test the distribution of clocks to multiple sources, using discrete RF components from ON Semiconductor[1] and the Samtec Firefly 12-channel TX multi-mode optical transmitters [2]. The architecture of the demonstrator distribution system is shown in Fig. 1. It was initially designed to supply a 160 MHz clock by distributing a 640 MHz clock and dividing the clock by a factor of four at the front end. This choice was made to stay within the specifications of the SFP optical transceivers, which are rated for 1 Gbps and above. However, we also used the system to demonstrate clock distributions at 40 and 160 MHz without the need for clock division. The system consisted of a set of three custom boards. These were:

[1] ON Semiconductor, Phoenix, AZ, USA

[2] Samtec, New Albany, IN

- **Clock 640** This board is a simple clock generator board that uses a Silicon Labs Si5344 [3] to generate a 640 MHz stable clock from a 40 MHz quartz oscillator.
- **Fly640** This board receives the clock on differential RF SMA connectors and fans them out to four 12-channel Firefly Tx modules. Thus from a single input, clock 48 copies of the clock can be distributed. The board is equipped with the ON Semiconductor Fanout, NB7VQ1006MMNG[4], which is rated for >7 GHz clocks.
- **FE640** This board is intended to mimic a front-end card. It has two ON Semiconductor flip-flops (NB7V52M) [5], which are rated for >10 GHz clocks, used to divide the clock signal by a factor of four.

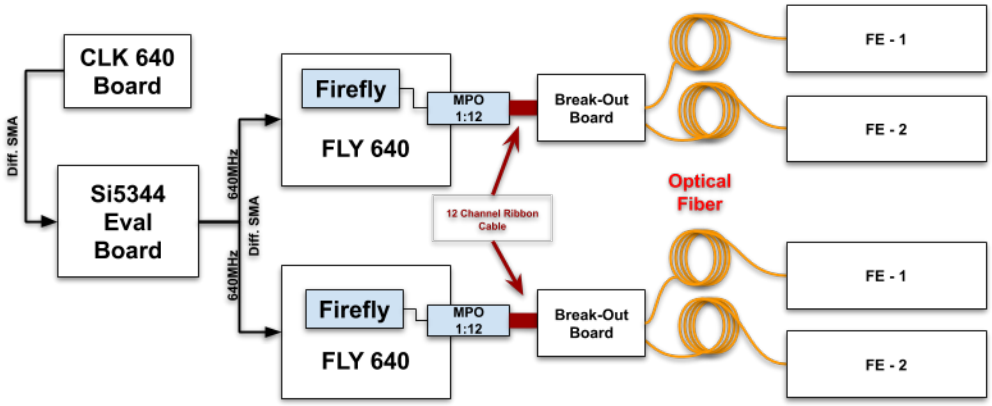


Figure 1: The demonstration system, showing the full set of boards designed for these tests. The Clock-640 board generates a 640 MHz digital clock signal. The Fly640 board receives the clock signal and distributes it to four 12-channel Samtec Firefly optical transmitters. The optical signal is sent via a long multi-mode fiber to a front-end emulator. The front-end emulator divides the clock by four and fans out the signal to twelve separate channels.

3. Measurements

We report here results from two measurements that were made using this system. These were the distribution of a 640 MHz clock with a divide-by-four at the front end, and the distribution of a high quality 160 MHz clock without division to a VTRx [1] optical receiver. Our measurements were made with a Microsemi 5125A Extended-Range Phase Noise and Allan Deviation Test Set and a custom Dual Digital Mean Time Difference (DDMTD) circuit [2, 3, 4], shown in Fig. 2. In the DDMTD circuit the choice of the frequency of the clock delivered by the PLL is chosen to be slightly offset from the the input clock by f/N Hz. Where f is the input clock frequency and N

[3] Si4344 data sheet
[4] NB7VQ1006MMM=NG data sheet
[5] NB7V52MMG data sheet

is an integer. For the measurements reported here, N was set to be 100,000. The outputs of the flip-flops are metastable, when the input and the offset clocks are aligned. By comparing the times of the metastablity for the two input clocks the mean phase variations between them can be found. For a 160 MHz clock with N = 100,000 the metastable state occurs with a frequency of 1.6 KHz. Thus the mean phase variation over these time intervals can be measured with high precision.

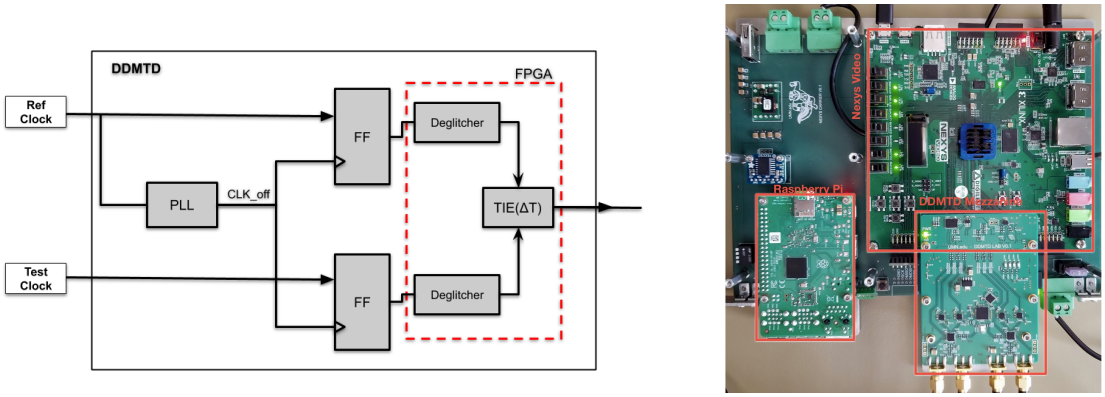


Figure 2: Diagram showing basic operation of the DDMTD circuit (left). In our application the flip-flops were the same ON-Semiconductor devises used in the demonstrator circuit. With the helper PLL frequency offset by 1/10,000, we can detect and measure wander between two clocks with a precision of ≈200 fs. The board (right) is connected to a Nexsys video card[5] through an FMC connector for readout.

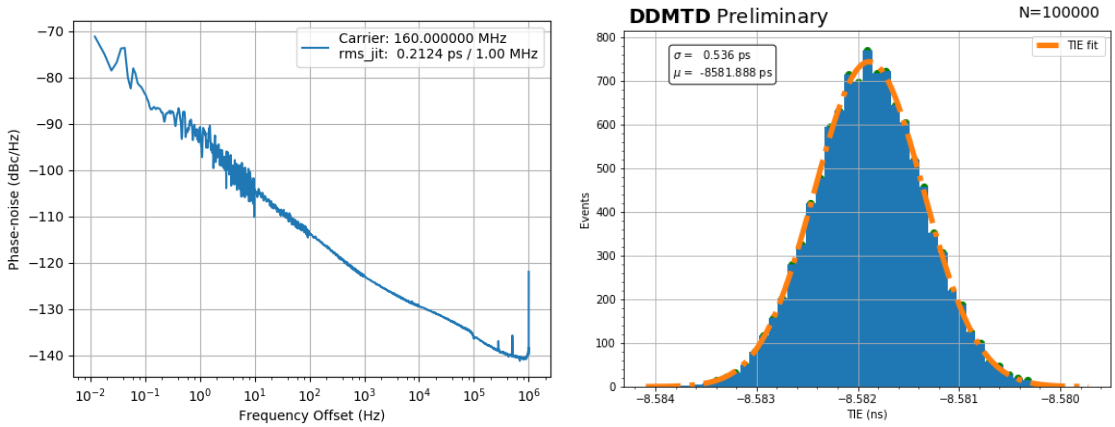
3.1 640/160 MHz distribution

To emulate the distribution of a 160 MHz clock to two separate regions of a detector, we injected a 640 MHz clock into two branches of the demonstrator system with 90 m of optical fiber between the FLY 640 boards and the FE 640 boards. The front-end emulator boards divided the 640 MHz clock down to 160 MHz.

We used the Microsemi 5125A Test Set to measure the relative phase noise between two 160 MHz clocks in two arms of our demonstrator system (top right and bottom right in Fig. 1). In the test we used one of the clocks as a reference and the second one as the test clock. The phase noise plot of this measurement is shown in the left plot of Fig. 3a and the integrated relative phase noise between the two output clocks was measured to be 0.21 ps in the interval of 0.01 Hz to 1 MHz. The measurement with the DDMTD of the mean time difference between the two clocks measured in an interval of 625μsec had a standard deviation of 0.53 ps, shown in Fig. 3b.

3.2 Direct Clock distribution

In a separate measurement we investigated the mean phase noise between two 160 MHz clocks. For this test, shown in Fig. 4, we used a high precision oven-controlled crystal oscillator coupled to a Si5344 PLL as a clock-cleaner to generate the source clock, which was input to a fan-out. From the fan-out two copies of the clock signal were sent to separate FLY640 boards, and then transmitted on two 90 m multimode fibers to VTRx optical receivers. The outputs of the VTRx were sent via SMA cables to a DDMTD, operating with $N = 100,000$. To set the noise floor of the



(a) Relative phase noise plot

(b) DDMTD measurement

Figure 3: Measurements comparing two 160 MHz output clocks from separate branches of the distribution system. Left: The phase noise between the two clocks integrating between 0.1 Hz and 1 MHz, which was measured to be 0.2 ps. Right: The mean phase variation between the clocks measured with the DDMTD with N = 100,000, or an interval of 6.25 μ sec, was found to be 0.53 ps.

measurement, two identical copies of the signal from the fan-out were input to the DDMTD, and the mean phase difference was measured to be 0.43 ps, shown in Fig. 5 (left). At the output of the VTRxs the relative phase was observed to have increased to 0.80 ps, as shown in Fig. 5 (right). In a similar measurement, where the VTRxs were replaced with SFP optical receivers, the measured phase noise was 0.71 ps,

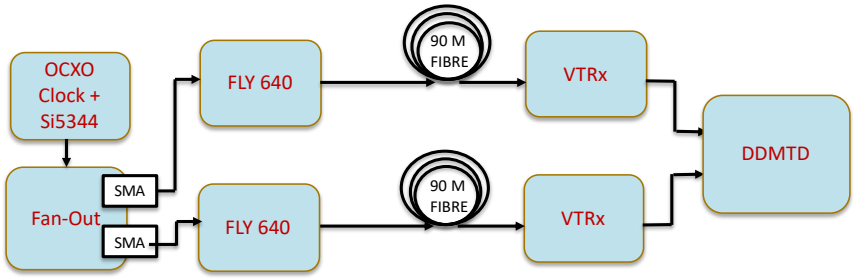
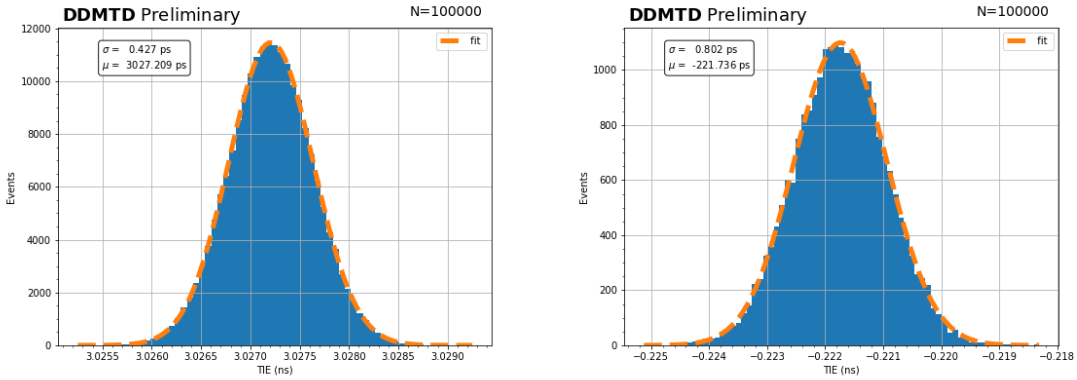


Figure 4: Setup used to measure the induced phase noise with 90 m optical fibers in each arm and VTRx optical receivers.

4. Summary

In this report we present results obtained in a study of a pure clock distribution system that we are investigating for use in the upgrade of the CMS detector for the HL-LHC. The relevant performance criterion for clocks distributed to particle detectors that are designed for precision timing measurements, is the phase noise between two separate channels in both the high- and low-frequency domains. To understand the level of precision that can be achieved, we have built a



(a) DDMTD Measurement at Fan-Out

(b) DDMTD measurement at the output of the VTRx

Figure 5: Measurements made with two 160 MHz output clocks from separate branches of the distribution system shown in Fig. 3. The plots show the mean time difference measured between clocks at the fan-out (left) and after the VTRxs (right). The former reflects the noise floor of the system at 0.4 ps, while the latter reflects the noise added in transmission and was 0.8 ps

demonstration clock distribution system using discrete RF integrated circuits. With this system we have demonstrated that it is possible to distribute a pure 160 MHz clock to separate detector components with a phase noise between the two clocks of ≈0.2 picoseconds, when integrated between 0.01 Hz and 1.0 MHz. With a digital dual mean time difference circuit we have measured the mean time difference over 625 μs to have a standard deviation of 0.53 picoseconds

5. Acknowledgments

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