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The powering concept of the Silicon Tracking System for CBM@FAIR

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A prototype powering chain of the Silicon Tracking System (STS) for the future CBM experiment at FAIR/Germany has been built. Low noise powering allows precise measurement of minimum ionising particles and its efficiency is an important task with the goal to minimise power dissipation and heat development. Also, the limited space for power cable routing has to be taken into account. Chosen solutions determine the necessary cooling and cabling effort and therefore have a high impact on system integration. Some aspects are already completely solved, while other issues have to be further investigated. The current status concerning powering the STS electronics and the consequences for system integration will be shown.

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1. General assumptions

Compressed Baryonic Matter (CBM) is a fixed target heavy ion physics experiment at FAIR/GSI in Darmstadt/Germany. To investigate the QGP phase diagram in region of high baryon-densities,

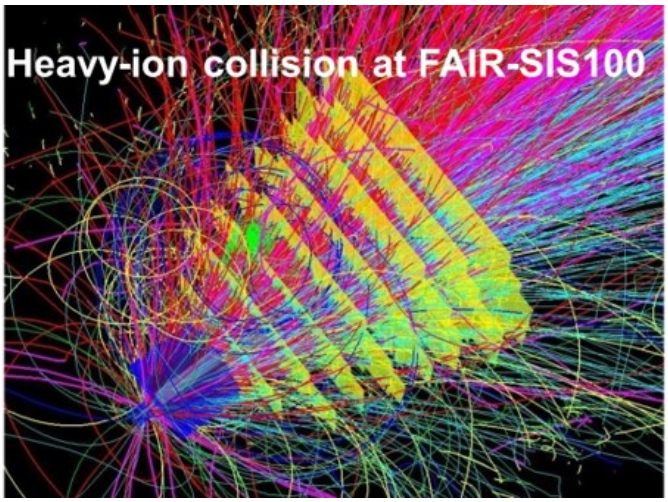

Figure 1: One Au-Au event simulated in the STS volume. The silicon sensors (yellow) of STS will be placed in a strong magnetic field of 1 T to allow for momentum measurement of the secondary particles via tracking of their curvature.

very high interaction rate measurements will be performed (up to 10^7/s (AA), up to 10^9/s (pA)). The STS, which is the main part of the CBM experiment, comprises nine units that build eight detector planes (Fig.1) installed in a thermal enclosure. Each STS-unit consists of two halves which

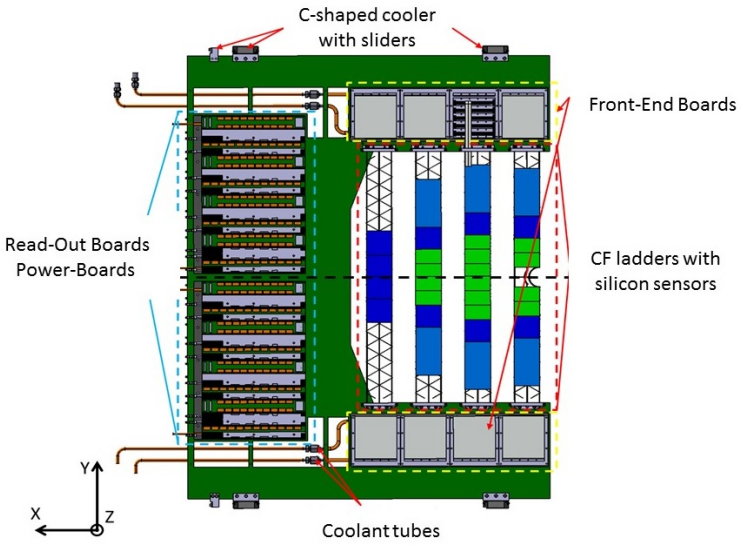

Figure 2: Silicon sensors, Front-End-Boards (FEBs, grey rectangular boxes), Read-Out-Boards (ROBs) and Power-Boards (PoBs) are mounted on the C-shaped cooling structure (green). One half of a STS unit is shown.

will independently of each other be supplied with low voltage LV, sensor biasing high voltage HV, optical fibers, cooling etc. The base structure of one half-unit is a C-shaped aluminium cooling plate (Fig. 2). Silicon strip detector signals are read out via micro-cables by corresponding read-out SMX ASICs (STS-MUCH-xyter [1] [2] [3]) located on Front End Boards (FEBs).

1.1 Electrical aspects

Silicon sensors need to be biased with +V and -V in a floating manner applied to p- and n-sides such, that the value of 2xV corresponds to the bias voltage actually applied. Conductors with maximum possible cross sections are used in the low voltage branch to minimize voltage drop over the supply cabling. This minimizes heat generation in the cabling, where it cannot be cooled efficiently. For the same reason, special attention is paid for sufficiently dimensioned traces on the PCBs involved.

Not to become the major noise contributor, the powering LDO should have an output power spectral density much lower than the electronics noise calculated to the power supply input port. The plot in Fig.3 shows the simulated noise spectrum calculated to the VDDM power pin, which

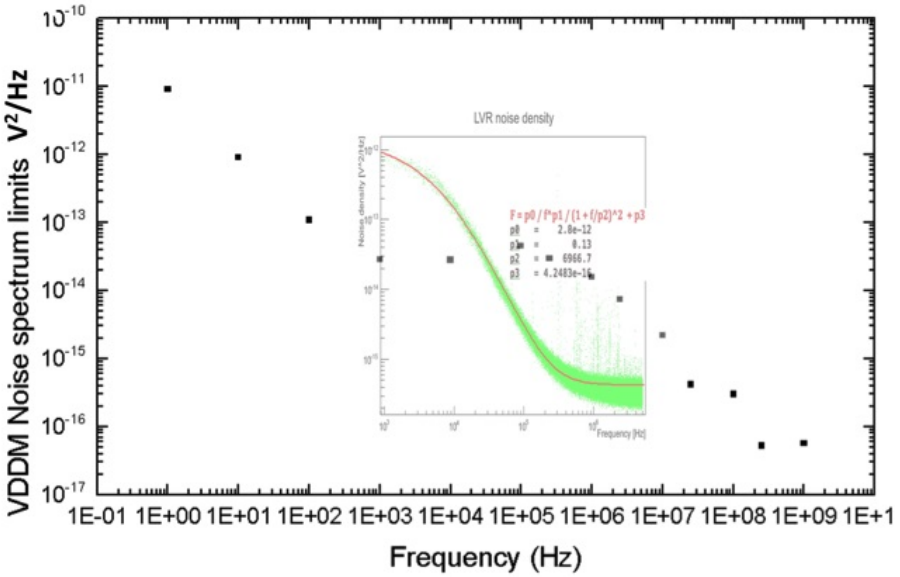

Figure 3: Required for SMX noise density spectrum (black dots): values well below 5x10^{-14} V^2/Hz have to be reached. Overlayed is a measurement of the output power spectral noise density of a sample LDO supplied by Semi-Conductor Laboratory, Nagar, India [5] and tested for CBM (green).

needs to be undermatched by the overlayed LVR noise density. For the respective frequency band (1kHz - 100MHz), the power-port related total electronics noise reaches value of approx 730 μV rms. The limiting noise value of of 70 μV RMS (10% of equivalent rms noise from the electronics itself) was accepted as the specification for the LDOs.

1.2 Thermal issues

The non-negligible heat amount produced by the buck converters (efficiency of 80% at most

for the air coil based FEAST MP) and the PoB itself is to be dissipated directly to an aluminium cooling block. Simple calculation shows (assuming that resistivity of the cables and connectors as well as voltage drop and power loss on the cables is known at nominal power consumption) 9.3W of power loss per FEB (8 STS-XYTER ASICs on one board) and 2.6W for each FEAST MP pair of converters.

2. Construction

2.1 LV and HV inside the STS-box

The 12 V DC @ 1 A from outside of the STS is converted to 1.2 V and 1.8 V for each FEB individually and 1.5 V and 2.5 V for the ROB on the side frame of the detector by FEAST MP boards [4]. One PoB PCB can serve up to 20 FEAST MP boards.

2.2 Low noise LDOs

A newly developed LDO from SCL India [5] (with a drop voltage of a maximum 0.4 V at output current of 1.3 A) are used in the final design. The size of the chips is 5 mm x 6 mm. These devices have a very low noise spectral density in the range from 100 kHz to 100 MHz (Fig.3).

2.3 Power dissipation in STS

Power dissipation reaches 6 W per FEB (FEASTs and LDOs only) and 0.2 W on LV cables. Multiplying these numbers by amount of FEBs one obtains almost 11000 W which is produced inside the STS box by low voltage powering infrastructure. Active cooling is necessary for the FEAST MP on the PoB and – wherever possible – for power cables. Aluminum active cooling shelves are used for FEBs and ROBs and partially for cables to reduce the heat transfer to the surrounding gas inside the STS box.

3. Noise results and summary

Measurements have been performed with the construction described above and a GBTx [6] based triggerless data acquisition system. Fig. 4 shows the equivalent noise charge measured for one SMX ASIC connected to a 6 x 6 cm^2 double-sided silicon sensor via 50 cm long micro-cable. The lowest achieved noise was 1150 e- rms. The alternating pattern in noise and larger values at the sides are attributed to the TAB bonding structure and imperfect shielding of the microcables in this mock-up assembly. Two channels 99 and 100 are damaged at the tab-bonding level.

The powering concept of the Silicon Tracking System in the CBM Experiment at FAIR was designed, constructed and tested in the conditions close to the final system. The ASICs are powered via full-custom voltage regulators (SCL India) supplied by rad-hard DC-DC converter (FEAST, CERN). The constructed demonstrators show that achieving targeted performance is feasible.

References

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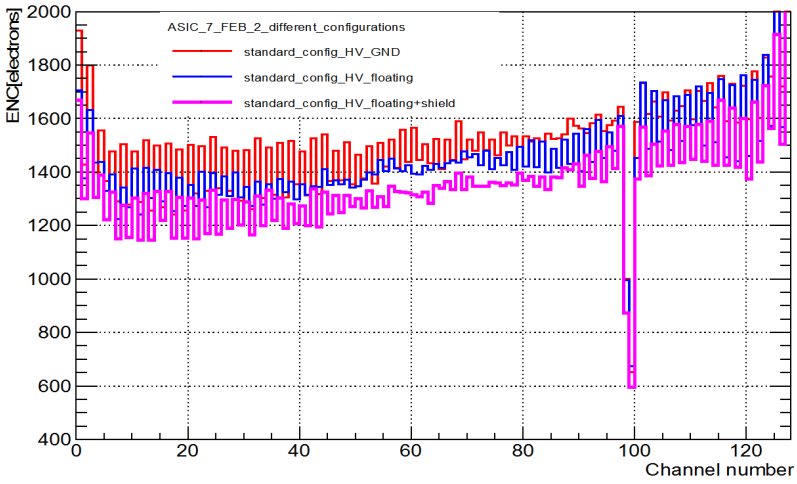

Figure 4: Equivalent noise charge of the system built with STS-XYTER, 6 x 6 cm^2 sensor and 50 cm micro-cable for different configurations of the high-voltage bias of the detector.

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