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A High Throughput Production Scale Front-End Hybrid Test System for the CMS Phase-2 Outer Tracker Upgrade

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Abstract

More than twenty-five thousand hybrids will be produced for the CMS Outer Tracker Phase-2 Upgrade. The hybrids are assembled with flip-chips, passives and carbon-fibre stiffeners. They will be glued to their module supports, together with powering and optical transmission hybrids, making repairs almost impossible. Due to the complexity of the hybrid circuits and the circuit assembly, production scale testing is a very important aspect. A crate-based scalable test system was designed to enable a multiplexed test of front-end hybrids. A test card was produced for the 2S hybrids and two different hybrid test cards are under development.

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1. Introduction

The new design of the CMS Outer Tracker is based on two main types of modules, the strip-strip (2S) and the pixel-strip (PS) modules [1]. These modules require state of the art High Density Interconnect (HDI) front-end hybrids assembled with fine pitch flip-chip front-end ASICs, connectors and passives [2]. All together 27900 2S type hybrids and 26960 PS type hybrids are required for the module constructions. The modules are assembled from several high value components glued together, making repairs almost impossible. Modules assembled with faulty hybrids are not repairable and have to be discarded. For this reason, the testing of hybrids before their integration into modules is essential. This paper describes the details of the test system design, shows the performance of the prototypes and introduces the future designs and plans.

2. Architecture of the test system

The test system consists of four main functional blocks: The test cards, the backplanes mounted in the crate, the FC7 FPGA board and the main test computer. The test cards are hosting the hybrids under test and do all the required signal transitions, measurements and power the hybrid. The backplanes are controlling the selection of test cards, distribute the main power rails and switch the high-speed signals to the appropriate signal path. The FC7 is controlling the hardware selection signals, provides the communication platform for the LVDS signals and some test functions are implemented in the firmware of the FPGA, but the data is mostly transferred to the main test computer for further processing. The main test computer runs the high level test routines, controls the selection of test cards and transfers the results to a database. The architecture of the test system is illustrated in Figure 1.

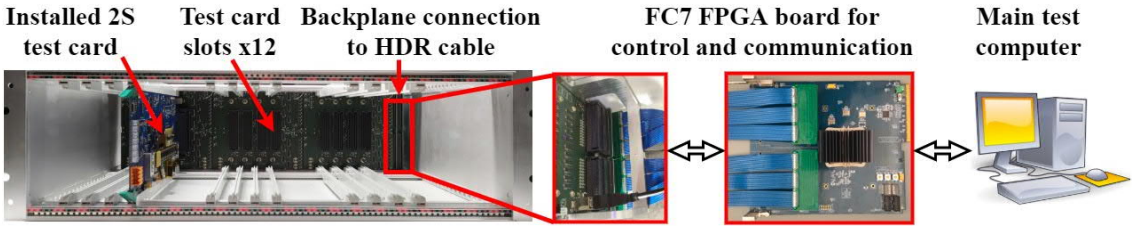

Figure 1: Architecture of the hybrid tes system.

The architecture of the test system was developed mainly around five key points that are explained in the following sub-sections.

2.1. High throughput to enable testing at manufacturers

The most important aspect during the design and specification phase of the test system was to provide high throughput. This is needed to enable electrical testing of the circuits after the assembly at the manufacturer premises. The most time consuming part of the testing is to mount the hybrid circuits on their sockets and to interconnect them to the test cards and, if the test is not done at room temperature, the time to reach the setpoint temperature in the climatic chamber. While the temperature of the climatic chamber is settling and the automatic electrical testing is running, the operator can mount the next batch of hybrids on test cards. Reading all the test cards in parallel is unnecessary and very resource intensive, therefore the test cards are multiplexed automatically by a custom designed high speed multiplexer backplane. Each crate assembly can host up to 12 test cards.

2.2. Scalability to reduce installation size at collaborating institutes

The size of a 3U Eurocrate compatible back-plane is around 420 x 130 mm^2. To allow downscaling the system at the collaborating institutes, where high throughput is not always required, the backplane is split into three Printed Circuit Board (PCB) sections. This allows for the installation of smaller-scale test setups with reduced space requirement and cost. In addition, the advantage of the split backplane is the reduced cost of repairs. In case of a failure, only one section of the backplane is replaced. Backplane sections are interconnected with right-angle Searay connectors mounted on the left and right board edges. On the first backplane of the chain, these connectors are used to connect to the FC7 FPGA [3] board, through Samtec HDR cables. The interconnected backplane sections mounted in a crate are illustrated in Figure 2.

Figure 2: Three backplane sections interconnected and assembled to form a full backplane.

2.3. Compatibility with already developed hardware and software

To keep compatibility with the test systems already developed for existing hybrid prototypes, the backplane is compatible with the FC7 board that is widely used by different CMS subsystems. The test card designs are compatible with the existing software tools as much as possible.

2.4. Versatility to support test cards for each hybrid type

In order to provide a versatile test system, which is capable of testing all the different types of hybrids, the backplane was designed to multiplex all the required high-speed IOs for the PS front-end hybrid (PS-FEH) test card, which is the most resource-demanding one. The backplane is multiplexing a USB link from the test computer and it distributes the 3.3V, -3.3V and 1.5V power rails. All the other hybrid-specific test functionalities are implemented on the dedicated test cards.

2.5. Usage of standard elements where possible

Reducing the design time and work was an important aspect during the design of the test system. The plug-in card connectors and their pin mapping are compliant with the VITA 57.1 standard Low Pin Count FMC (LPC) connector definition. This provides the possibility to design test cards that can be operated in stand-alone mode being connected directly with an FMC interface. This feature eliminates the need for an additional desktop test card design. Usage of standard crate assemblies and Samtec HDR cables were all choices reducing the amount of customization.

3. Backplane design and component validation

The backplane design relies on a careful selection of components and architecture. Several components were considered in different architectures such as cross-point switches, 4:1 multiplexers in a bus architecture and 2:1 multiplexers in a tree architecture. From these options

the tree architecture with 2:1 multiplexers was the easiest in layout and required the least amount of components. The architecture for backplane inputs is illustrated in Figure 3. The selected analogue multiplexer is the TS3DV642 with 12 channels. Each LVDS input signal is buffered with devices from the DS25BR family. The analogue multiplexers and the buffers were tested on their evaluation boards before the design started and their performance was sufficient to be included in a design with signal bandwidths up to 1.28 GHz. The PCB of the backplane is a 12 layer stack with blind and buried microvias and controlled impedance transmission lines. Each backplane has four vertical Searay connectors on the back side, interconnecting the test cards.

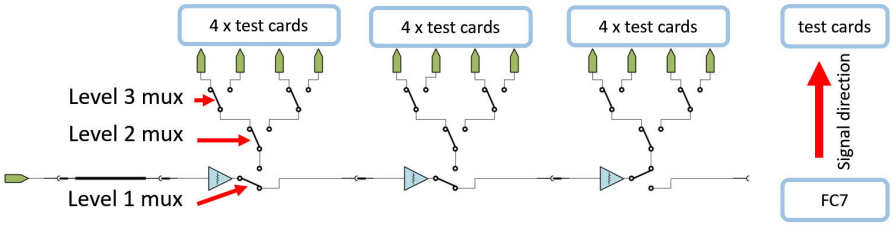

Figure 3: The selected tree type backplane multiplexing architecture for inputs.

4. Test card designs

Currently the 2S test card is already prototyped and being used with the test system. Two additional cards are being designed: the PS-FEH test card and the PS-ROH test card. These test cards share the same geometry for the card outline and the connector placement. The functions are also similar: signal level translation, buffering, analogue to digital conversion and other tests to qualify the hybrids [5]. The PS-FEH test card has additional complexity as it includes also a spring loaded needle test socket with mechanical structures pressing the hybrids onto the socket. A prototype 2S test card with an 8CBC3 hybrid is illustrated in Figure 4.

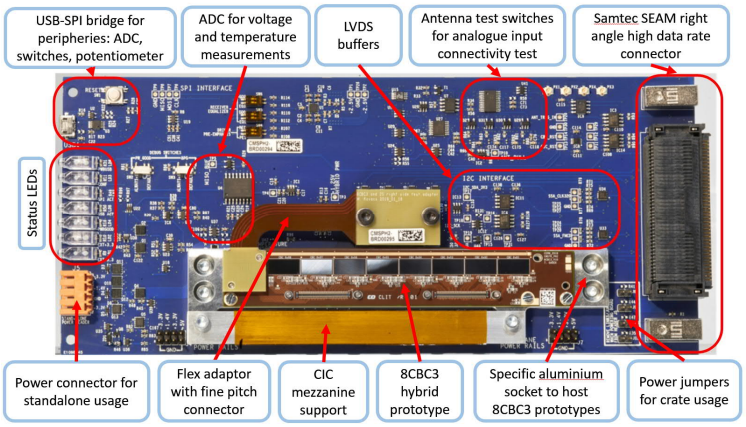

Figure 4: Functional blocks of the 2S hybrid test card mounted with 8CBC3 front-end hybrid under test.

5. Performance of the test system

The performance of the test system was measured first without test cards and later with test cards connected to the backplanes. The measurement without test cards was performed with three backplane modules interconnected. In this case the scattering (S) parameters were measured and post processed. The results show excellent signal performance up to 1.28 Gbps. This is in line with the preliminary component measurements described in section 3. The highest bandwidth required for the PS-FEH testing is 640 MHz, therefore this result fulfils the specifications of the system. The measurement setup and result is illustrated in Figure 5. The second set of measurements included also the 2S test cards. A test card was inserted into all the slots of the backplanes and phase alignment and word alignment procedures were performed on the data lines

connecting the hybrid front-end chips to the concentrator chip (CIC). Front-end calibration, register test and data error check were performed after the phase alignment step.

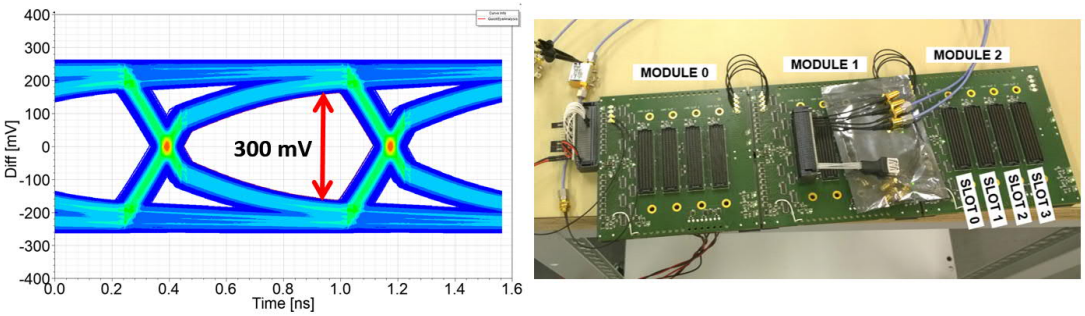

Figure 5: Simulated eye diagram (left) using the S parameters measured with the setup on the right.

All the functions of the backplanes worked correctly with the 2S test cards in every slot and all the front-end hybrid tests provided identical results. The eye diagram of the 320 MHz clock signal was measured on the 2S test card and showed a good signal quality with large eye opening. The measurement setup and the eye diagram are illustrated in Figure 6.

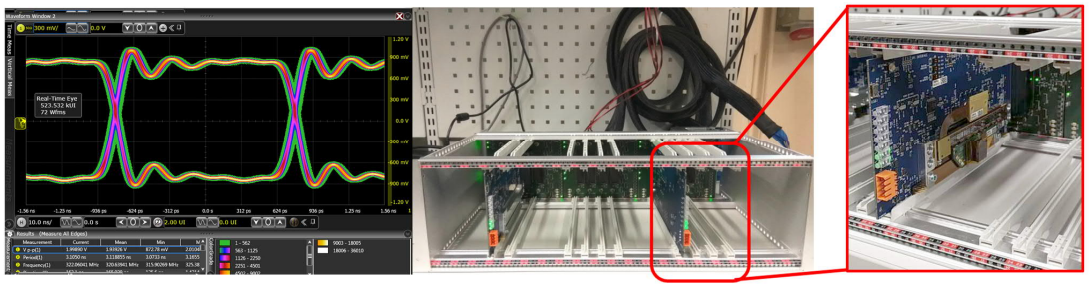

Figure 6: Eye diagram of the 320 MHz clock output of the 2S test card connected to the backplanes.

6. Summary, conclusions and future work

A high throughput front-end hybrid test system was developed for the testing needs of the CMS Outer Tracker Phase-2 Upgrade. Many design aspects were considered during the design: high throughput, scalability, versatility, compatibility and usage of standard components. The system was tested with and without the 2S test cards and the test results confirmed the correct operation of the backplane cards, the firmware and the control software. The multiplexing is transparent for the front-end hybrid test software and test results are identical in each slot. New test cards are currently under development for the PS-FEH and PS-ROH hybrids. Evaluation work and software development will continue with the new test cards, including long term reliability testing and high and low-temperature operation.

References

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