PROCEEDINGS OF SCIENCE

Readiness of the ATLAS Tile Calorimeter link daughterboard for the High-Luminosity LHC era

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The Daughterboard (DB) is the read-out link and control board that interfaces the on- and off-detector electronics for the High-Luminosity Large Hadron Collider (HL-LHC) of the the ATLAS Tile Calorimeter (TileCal). The DB sends high-speed read-out of digitized Photomultiplier (PMT) samples, while receiving and distributing configuration, control and LHC timing. A redundant design based on Xilinx Soft Error Mitigation (SEM), Triple Mode Redundancy (TMR), Forward Error Correction (FEC) and CRC Cyclic Redundancy Check (CRC) strategies minimizes single failure points while withstanding single-event upsets and damage from minimum ionizing and hadronic radiation. We present the current results of the performed TID, NIEL and SEU tests, aiming to demonstrate the readiness of the Daughterboard to satisfy the radiation requirements imposed by the HL-LHC.

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1. HL-LHC and the ATLAS Tile Calorimeter

The five fold increase of instantaneous luminosity at the HL-LHC will impose higher radiation levels and increased rates of pile-up to the read-out systems of the ATLAS detector (Figure 1a) [1]. The ATLAS Tile Calorimeter (TileCal, Figure 1b) is a sampling calorimeter composed by plastic scintillator tiles and steel plates that act as active and absorber materials, respectively. Four cylindrical barrels (Figure 1c) are each sliced into 64 wedge-shaped modules (Figure 1d). Light produced by the scintillators is collected by wavelength shifting fibers and read out by PMTs.

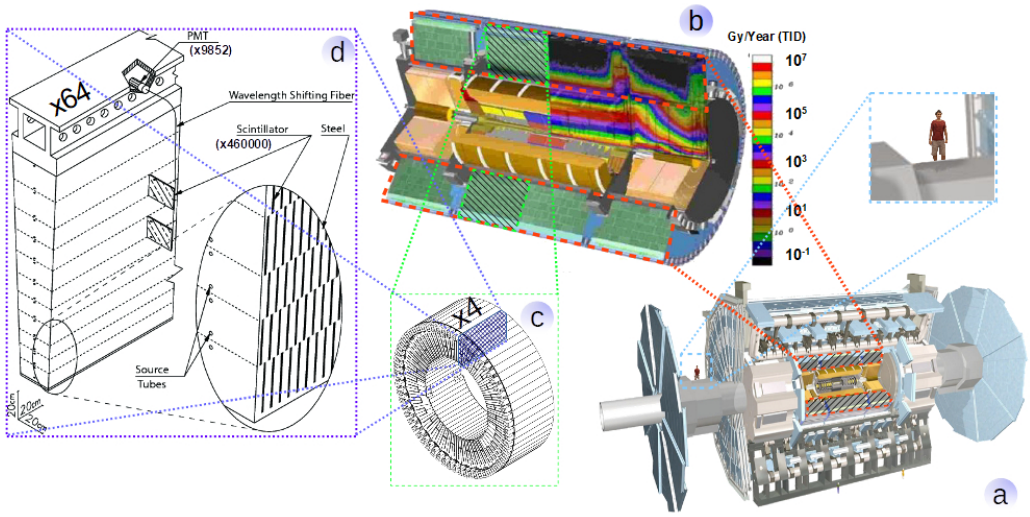

Figure 1: (a) The ATLAS detector. (b) Tilecal and the inner detectors. (c) A TileCal barrel. (d) Depiction of a TileCal wedge-shaped module.

The present read-out electronics of TileCal are incapable of coping with the HL-LHC requirements. Hence, Tilecal's on-detector and off-detector electronics will be fully replaced with a design that will provide continuous full digital read-out with better timing, better energy resolution and less sensitivity to out-of-time pileup [2]. All the on-detector developed hardware require Total Ionizing Dose (TID), Non Ionizing Energy Loss (NIEL) and Single Event Effects (SEE) tests to qualify the design to meet the HL-LHC conditions.

2. TileCal read-out system for the HL-LHC

The TileCal HL-LHC on-detector read-out electronics will be positioned in the wedge girders and will be mechanically divided in modules, so called Minidrawers (MD). Each MD houses electronics that services up to 12 PMT channels (Figure 2a). Each PMT signal is conditioned, shaped and fed into high-gain and low-gain circuitries in a Front-end electronics (FENICS) card. A mainboard (MB) digitizes all the conditioned signals of a MD at 40 MHz and sends it to a link Daughterboard (DB, Figure 2b). The DB receives and propagates LHC synchronized timing, control and configuration to the front-end, while transmitting continuous read-out of the MB channels to the off-detector systems (Figure 2c). On the off-detector, a Tile Preprocessor (TilePPr) continuously receives and stores the two gains of PMT data in pipelines until a reception of a trigger decision event, while providing processed reconstructed data to the trigger system.

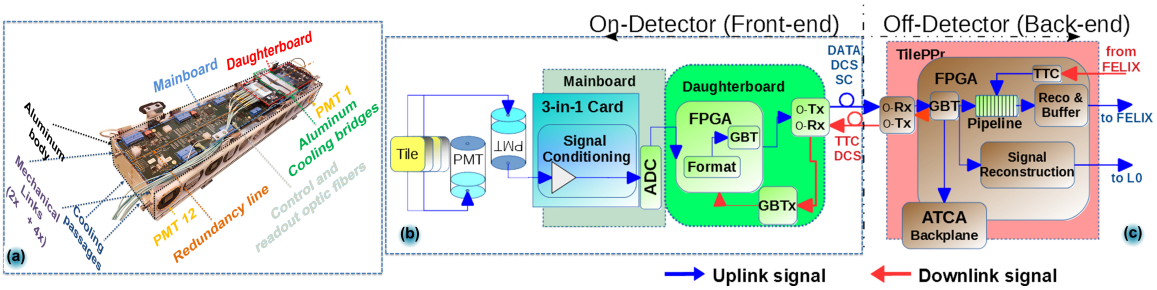

Figure 2: TileCal HL-LHC Upgrade read-out system: (a) TileCal HL-LHC Upgrade Minidrawer, (b) On-Detector electronics block diagram and (c) Off-Detector electronics block diagram.

3. The Daughterboard Revision 5

The DB Revision 5 (DB 5, Figure 3) is a read-out link and control board designed to fit the HL-LHC radiation environment [3]. The board is split in two equal halves, each independently powered, with redundant input and output links. The DB is interconnected with the TilePPr by means of two RX and four TX optical fiber links powered by four SFP+ modules. The DB interfaces the off-detector systems with the MB through a dense FMC connector. Additionally the DB provides interface to a high voltage control board (HV-OPTO), external analog sensors and the Cesium calibration system.

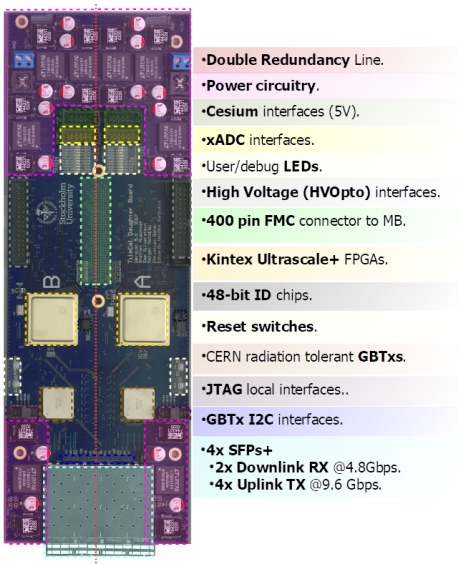

Figure 3: DB 5 main components.

The downlink is handled by two RX links running at 4.8 Gbps to drive a pair of CERN designed GBTx ASICs [4]. Each GBTx chip recovers LHC synchronized clocks to drive the transceivers of both FPGAs, the FPGAs relevant logic and the digitizing blocks on each MD quadrant. Additionally, each GBTx distributes synchronous and asynchronous control and configuration commands to both FPGAs and provides off-detector control of both FPGA reset signals and JTAG chains. Through the uplink, GBT-CRC protected words are continuously transmitted to the back-end through two redundant read-out links running at 9.6 Gbps each. The uplink words are formatted by a TMR protected FPGA firmware and contain two gains of digitized PMT data and slow control (SC) monitoring information. The DB 5 was tested for TID, NIEL and SEE. All the radiation tests included the DB 5 and two pairs of different SFP+ types: CORETEK CT-000NPP-SB1L-D (baseline) and AVAGO AFBR-709SM.

4. TID radiation tests

The DB 5 proved to withstand up to 20 kRad of TID with stable voltages, currents and temperatures over the whole irradiated dose (Figure 4 a and b). This was sufficient to qualify it for the HL-LHC lifetime within the radiation doses simulated as reported in the ATLAS Tile Calorimeter

Phase-II Upgrade Technical Design Report [2]. However, newer simulations performed with new geometry parameters dictate that to qualify the board, either a TID test should be done up to either 72 kRad or to 14.4 kRad if the test includes annealing.

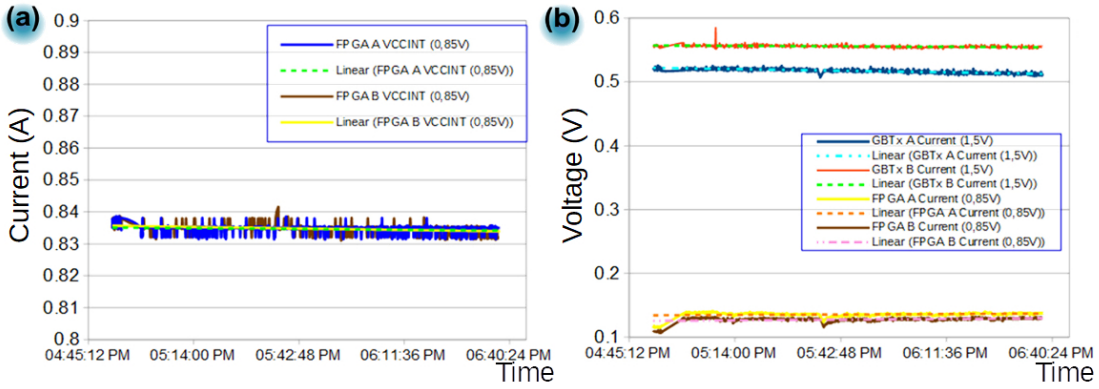

Figure 4: DB 5 TID test results for a board exposed to a total dose of 20 kRad. (a) shows the voltages of both DB FPGAs and (b) shows the currents of both DB FPGAs and both DB GBTxs, all over the full time of exposure.

5. NIEL radiation tests

The NIEL test was performed with a 52 MeV proton beam at the Institute of Nuclear Physics in Krakow. The target fluence was achieved at the expense of exposing the board to 768.2 kRad of equivalent TID, rendering the test inconclusive. Hence, the NIEL test needs to be re-done in a facility capable of achieving the target fluence of 9.00×10^{12} neutrons $\times \text{cm}^{-2}$ with neutrons. Two SFP+ candidates were tested with the DB. After exposure, the AVAGO SFP+ transceivers failed to work, while the Coretek SFP+ planned for the design baseline were fully functional the without noticeable performance losses.

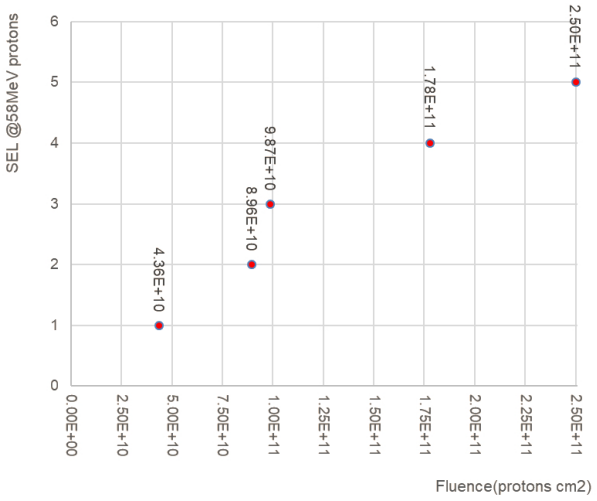

Figure 5: DB 5 SELs detected at 58 MeV proton beam that account for the data losses shown in Figure 6.

6. SEE radiation tests

The SEE tests showed that the Kintex Ultrascale+ 16 nm FinFET technology is susceptible to Single Event Latch-up (SEL) occurrences (Figure 5), with SEL-fluence rate increased from 2×10^{-11} SEL-fluence rate at 58 MeV to 2.36×10^{-10} rate at 226 MeV protons. The over-currents due to the latch-ups did not cause any noticeable damage, however SELs are highly undesirable.

The Single Event Upset (SEU) tests resulted in 4934 SEUs over a fluence of 2.05×10^{11} protons cm^{-2} (Figure 6), of which only 11 SEUs could not be corrected by the Xilinx Soft Error Mitigation (SEM). The SEM uncorrectable SEU rates predict that 1.4 $\pm$0.4 SEM uncorrectable errors are expected per Daughterboard per year. It is anticipated that the Xilinx SEM and the TMR will mitigate for both correctable and uncorrectable error rates without affecting nominal runs.

7. Conclusions

The DB 5 design aims to meet all the HL-LHC requirements. The board successfully passed the preliminary TID radiation tests, however new simulation results require a new test to be done with a new target dose. The NIEL tests could only qualify the CORETEK SFP+ transceiver and new NIEL tests are planned using neutrons instead of protons to reduce the ionizing dose. The Kintex Ultrascale+ 16 nm FinFET technology delivers a unacceptable SEL rates for the HL-LHC. Migrating to a SEL-resistant FPGA is needed to eliminate the occurrence of SELs in the DB. The board will be redesigned with an Ultrascale family FPGA, powered by 20 nm TSMC planar technology, where SELs have not been observed [5]. Using the Ultrascale family will increase the SEU rate by a factor of approximately 16 [6]; however, TMR and SEM will render most of these errors harmless for nominal runs.

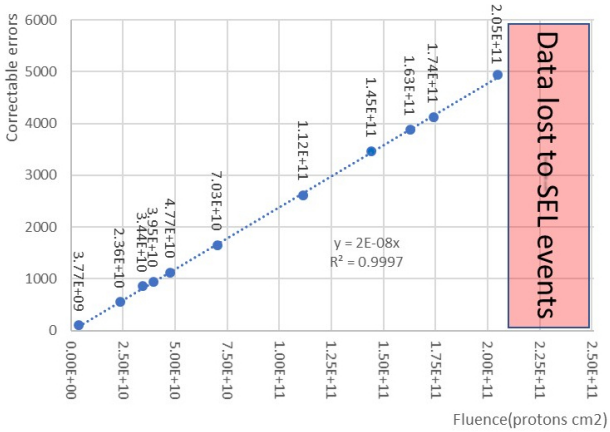

Figure 6: DB 5 SEU test. Each point shows the SEM correctable errors occurred up to a SEM uncorrectable error occurrence. About 0.45×10^{11} protons cm^{-2} of correctable error rates were lost due to the 5 unexpected SEL events shown in Figure 5a.

References

[1] ATLAS Collaboration, 2008 JINST 3 S08003.

[2] ATLAS collaboration. Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter. CERN-LHCC-2017-019, ATLAS-TDR-028, 2018.

[3] ATLAS Tile Calorimeter Link Daughterboard, PoS Volume 343 - Topical Workshop on Electronics for Particle Physics (TWEPP2018), DOI: 10.22323/1.343.0024.

[4] GBTX Manual, https://espace.cern.ch/GBT-Project/GBTX/Manuals/gbtxManual.pdf, 2016.

[5] Single-Event Latch-Up: Increased Sensitivity From Planar to FinFET, 2017 IEEE Radiation, IEEE Transactions on Nuclear Science 2018, DOI: 10.1109/TNS.2017.2779831.

[6] Single Event Upset Characterization of the Zynq UltraScale+ MPSoC Using Proton Irradiation, 2017 IEEE Radiation Effects Data Workshop (REDW), DOI: 10.1109/NSREC.2017.8115448.