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Multi-channel time-tagging module for fast-timing resistive plate chamber detectors

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A multi-channel time-tagging module is proposed for fast timing resistive plate chamber (RPC) detectors. It has been designed and implemented in a low-end and low-power cyclone V FPGA. Each channel mainly consists of a time-to-digital converter (TDC) in tapped-delay-line (TDL) architecture. The TDC has three main building blocks: tapped delay line (with registers and a AND logic), fine timestamp converter, and coarse timestamp generator. Several data processing techniques, including prior signal reshaping and noise-immune processing, have been adopted to minimize noise effects. The module has successfully been tested in all-channel simultaneous operation conditions, with 11 ps to 20 ps time resolution and full event-detecting efficiency for all the channels.

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1. Introduction

A new generation of Resistive Plate Chamber (RPC) detectors have been recently proposed to be equip two of the high η muon CMS detector stations [1, 2] for high-luminosity large hadron collider (HL-LHC) phase. Such a RPC requires multi-channel readout and precise time-tagging operation with low power consumption for the associated electronics. For this purpose, we have designed a multi-channel time-tagging module implemented using a low-cost, low-power Cyclone V GT FPGA. The module design needs to fulfil the following specifications: up to 56 channels, a full event-detecting efficiency, up to 16-channal simultaneous measurements, a dead time between successive measurements less than 10 ns and a time resolution less than 60 ps (Root Mean Square (RMS)).

The module requires a large number of delay elements and registers to be integrated in the FPGA. They could toggle simultaneously at the clock's rising edge. This simultaneous toggling operation involving large-scale elements in a small area could induce Ground Bounce and Voltage (power supply) Sagging (GBVS) [3]. The GBVS issue is more serious in a low-power and narrow-wiring FPGA. Furthermore, for simultaneous multichannel operation, the GBVS is a source of interferences. The GBVS could corrupt the delay elements' states, called bubble noise (i.e. bits with inverse value ahead and after) and temporally slow down signal transition time (due to power supply voltage fluctuations). Consequently, it degrades the accuracy of time-tagging measurements and produces error of event detection.

To deal with this issue, we have adopted several techniques, including prior signal reshaping and integration of noise-immune data processing in an encoder. A 56-channel time-tagging module has been designed and tested. Its architecture and operation will be described in Section 2. Section 3 will present testing and analyse, and Section 4 is for results and discussion.

2. Architecture and operation

The module mainly consists of 56 channels, each using a TDC in tapped-delay-line (TDL) architecture [4, 5]. Fig. 1 shows the architecture of our proposed TDL TDC. It basically consists of three blocks: tapped delay line (with registers and a AND logic), fine timestamp converter, and coarse timestamp generator.

The tapped delay line is built by using Adaptive Logic Module (ALM) in arithmetic mode as delay element with an average delay time of 5 ps on Cyclone V FPGA (at 25°c). It consists of 640 delay elements in carry-in/out serial connections, which gives a total delay time of 3.2 ns. The number of delay elements has been chosen for the total delay time to exceed one clock period, i.e. 2.5 ns, so as to ensure that the propagating signal is still on the delay line for registering at clock tick. It also includes an array of D-type flip-flop (DFF) registers to record the signal status in the delay line (640 bits). The registed signal status is known as thermometer code [7]. The array is followed by a 4-to-1-bit AND logic to reduce the length of thermometer code, so as to reduce the VSGB effect at the expense of measuring precision. Due to increased average delay time of each code from 5 ps to 20 ps, the resultant precision is degraded, but still acceptable for the requirement (below 60 ps). The output signal status becomes length-reduced thermometer code (160 bits). The tapped delay line block also integrates a signal-reshaping circuit [6] to shorten signal's transition time before its injection into the delay line and block the loop-back VSGB noise. It consists of a XOR logic and a high fan-out DFF in close loop to be configured as toggle

flip-flop, as shown in Fig. 2a. The high fan-out DFF has higher driving capability for output connection with large parasitic capacitance. This circuit reduces GBVS noise thanks to flip-flop operation. Input and output signal waveforms of the circuit are illustrated in Fig. 2b.

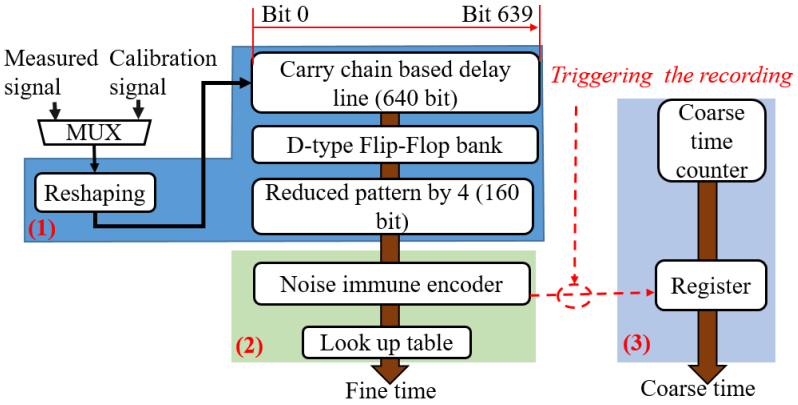


Figure 1: the proposed tapped-delay-line TDC consists of three blocks: (1) tapped delay line (with registers and a AND logic), (2) fine timestamp converter, (3) coarse timestamp generator.

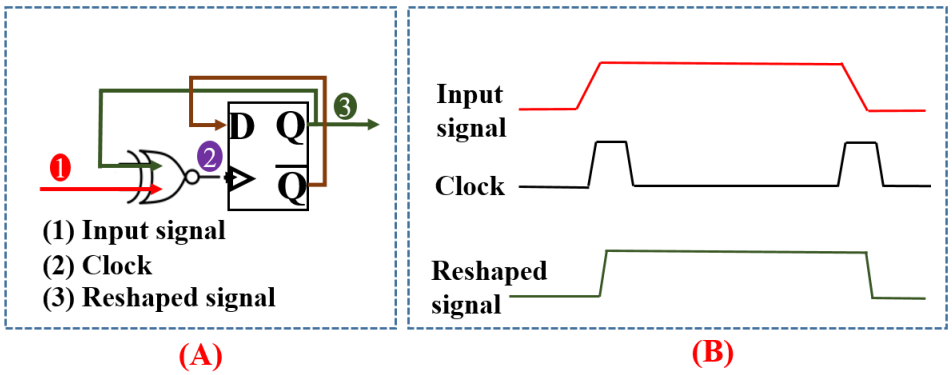


Figure 2: (a) signal reshaping circuit; (b) input and output signal waveforms of the circuit

The fine timestamp converter is mainly composed of a noise-immune encoder and a look-up table (LUT). The noise-immune encoder detects the signal's leading edge of the reduced status vector (length-reduced thermometer code) from the delay line block, and determines its position in the code. The position is then converted into fine time by using the LUT.

The noise-immune encoder is designed to tackle interference noise between channels. In practical, we have observed that interference noise corrupts the recorded signal status with changes of individual bits (called bubble bits). The recorded signal status with interference noise as well as leading edge detection is illustrated in Fig. 3. It consists in processing the output length-reduced signal using a 5-bit running window to detect leading edge. When the window exhibits [1][0][X][0][0], the result indicates that it is entering the transition area, and an hot-code output signal indicating the leading edge position is generated.

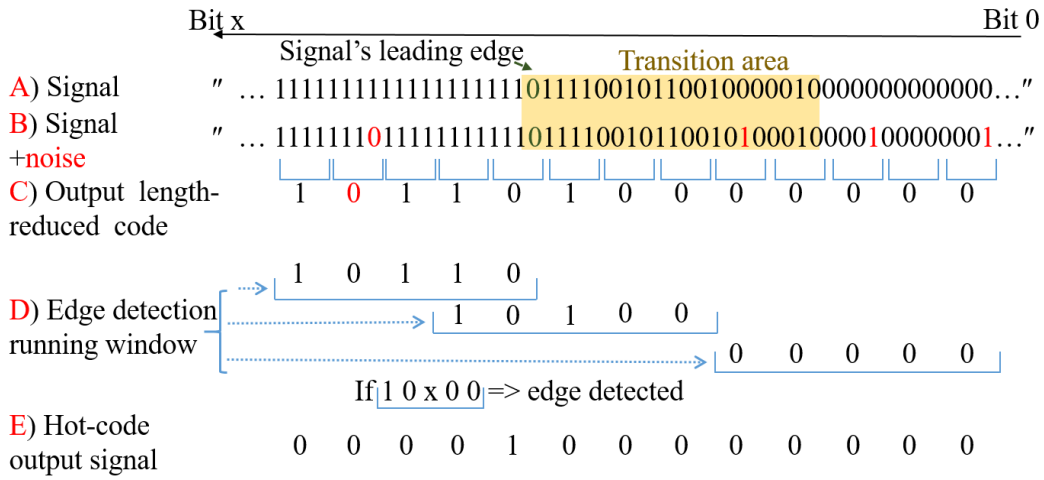


Figure 3: A) thermometer code without noise bit; B) thermometer code with noise bits; C) output length-reduced thermometer code; D) edge detection running window; E) hot-code output signal.

The coarse timestamp generator of the TDC consists of a 24-bit free-running coarse-time-counter, a 24-bit register. The 24-bit register is triggered by the detected signal from the fine timestamp converter to record the value of the coarse-time-counter as the corresponding coarse timestamp.

The TDC has two multiplexed inputs, one for calibration (with data recording in the LUT), and the other for normal operation.

3. Testing and analysis

The 56-channel time-tagging module has been tested using a 64-channel readout board with slow-control-and-signal-acquisition (Fig 4.a). Via an Ethernet link, the readout board is connected to a PC.

For the testing, a periodic pulse signal from a wave generator Keysight 81150A is injected to all the channels of the module. The injected signal has no correlation with the module's clock signals. Its detection in each TDC triggers the recording of both coarse and fine timestamps, and data are then transmitted to PC.

The time resolution of the TDCs has been evaluated by comparing output timestamp between two randomly-chosen channels and determining their difference. This signal subtraction eliminates jitter effect of the injected input pulse (because both channels are applied with the same pulsed signal with jitter, and the difference between their outputs cancels jitter effect). For a large number of pulses, the RMS of the timestamp difference is determined. Dividing the RMS value by $\sqrt{2}$ gives approximately the time resolution in RMS value for one channel. This measuring process is repeated to cover all the channels.

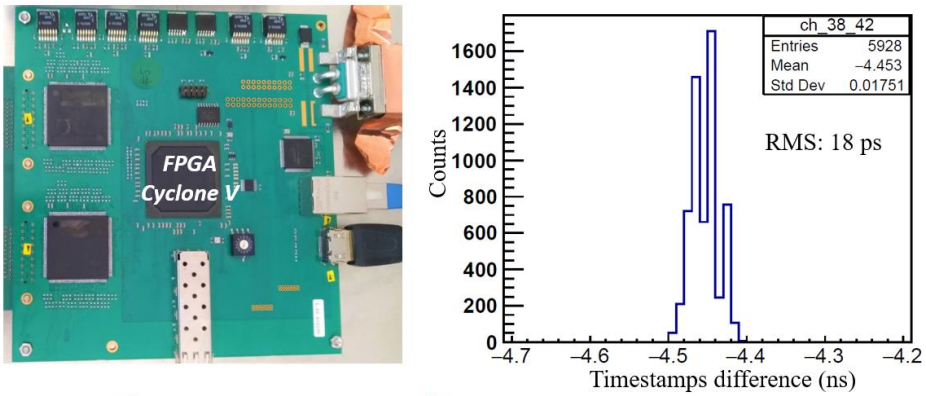
On the other hand, the detecting efficiency of the implemented TDCs has been evaluated by comparing the receiving event number of each channel to the reference event number.

4. Results and discussion

Fig 4.b shows statistical distributions of the measured timestamp difference between channel 38 and channel 42, which gives 18 ps in RMS. This corresponds to a time resolution of 12 ps for

these two channels. For all the 56 channels, the measured time resolution in RMS varies from 11 ps to 20 ps.

A 100% detecting efficiency for each channel has been evaluated.



A) Readout Board B) Timestamps difference between two channels

Figure 4: (a) readout board for testing the multichannel time-tagging module implemented in a Cyclone V GT FPGA; (b) statistical distributions of measured timestamp difference between channel 38 and channel 42.

5. Conclusion

We have designed a 56-channel time-tagging module implemented on a FPGA (Cyclone V GT device, 5CGT–D9-C7N) for RPC detectors. Each channel integrates a TDC with implementation of several data processing techniques to improve time resolution and detecting efficiency. Testing results show a time resolution of 11 ps to 20 ps in RMS for different channels, and a 100% detecting efficiency for all channels.

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