PROCEEDINGS OF SCIENCE

Back-end firmware for the LHCb VELO upgrade phase I

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LHCb is a general purpose experiment instrumented in the forward region at the LHC, specialized in b- and c- physics, new physics and CP violation. The vertex locator (VELO) detector is being upgraded along with the rest of the tracking system and readout architecture during 2019-2020. The aim of this paper is to present the architecture of the control and readout firmware on the VELO specific back-end boards.

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1. LHCb VELO upgrade

LHCb is a dedicated experiment searching for new physics by studying CP violation and rare decays of b and c quarks located in the LHC ring. The LHCb collaboration plans to change key features of the present detectors for Run III, moving to a full detector readout at 40MHz and operating at a luminosity of $2x10^{33}cm^{-2}s^{-1}$. The new readout scheme and operation conditions will require the replacement of many sub-detectors, one of them is the VErtex LOcator (VELO). VELO is the primary tracking and vertex detector that surrounds the interaction point. It will use hybrid pixel detectors ($55\,\mu$m $\times$ $55\,\mu$m pitch) composed of silicon sensors bump-bonded to a dedicated readout chip, VeloPix [1].

The whole VELO will be composed by 52 modules with 4 hybrid pixel detectors each (Figure 1). They are mounted in a mechanical frame capable of moving the sensors away from the interaction point when LHC beam is not stable. The control of the VeloPix ASICs is done over two multipurpose radiation tolerant bidirectional link ASICs (GBTx) [2] running with the CERN standard GBT protocol at 4.8 Gb/s. Front-end data acquisition links are driven from the VeloPix ASIC over almost one meter length copper transmission lines, converted into optical and sent out to the back-end readout boards.

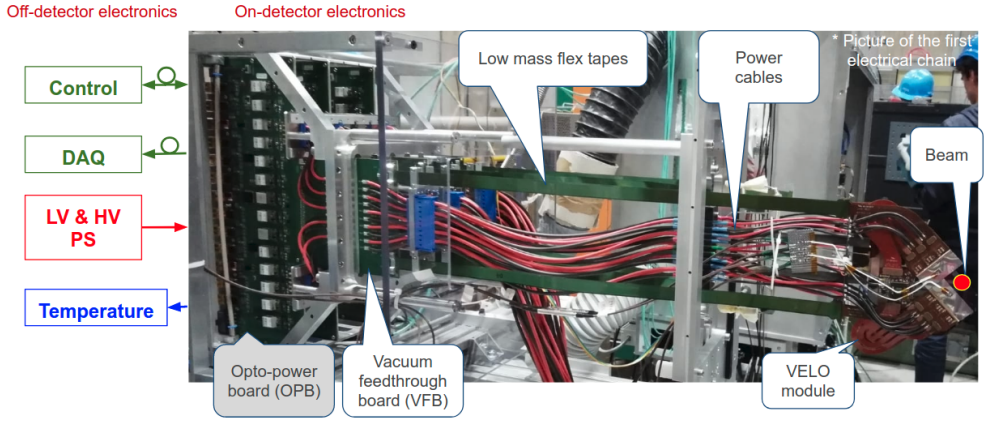

Figure 1: Slice view of a VELO upgrade.

2. VELO firmware

A single back-end board design, common for all the LHCb subdetectors and based on the Intel Arria 10 FPGA [3], named PCIe40 [4], is assigned to act as a supervisor, control and readout board. The functionality of the PCIe40 is defined by the firmware flavour. The PCIe40 board will be controlled and read out from a PCI express slot in a server placed in the LHCb area, at the ground level.

The firmware design shares common functionalities for all LHCb, for example the physical layer communication and the integration of the different parts of the system. Hence a common experiment wide development is being made, being in charge of every sub-detector group the modifications related to their specificities.

2.1 Control and timing

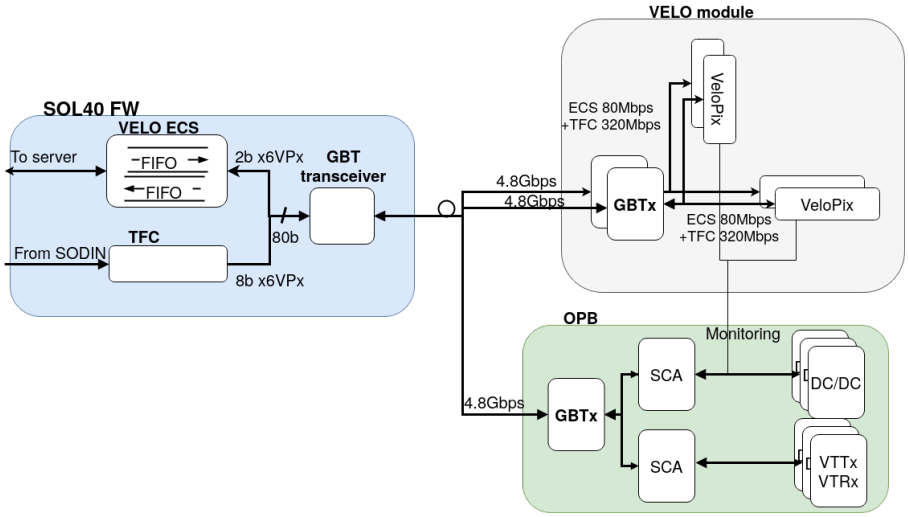

Figure 2: Schematic view of the control firmware for the VELO Interface boards (SOL40) distributing the control and timing signals to the front-end.

LHCb sub detector front-ends are controlled in a centralized way. In order to control the front-end electronics, a series of read/write registers in the PCIe40 boards that controls the hardware are accessed from a server that interfaces with the different SCADAs. In the case of VELO front-end ASICs the communication with the server is done by a FIFO memory with 32b bus. The interface between this FIFO and the front-end is done by serializing the command word at 80Mb/s and encapsulating it in a GBT frame that goes directly to the GBTx ASIC in the module. Maintaining the front-end ASICs synchronous with the rest of the LHCb experiment is a key part of this firmware, and it is done with the so-called timing commands. VELO 's firmware receives timing commands from the centralized LHCb readout supervisor board (SODIN) and encapsulate them into the same GBT word shared with the control signals and send it to the front-end GBTx ASIC who distributes them to the corresponding VeloPix ASIC.

2.2 Readout

The VELO readout board firmware is almost a full modification of the common LHCb framework as the VeloPix ASIC is the only LHCb front-end reading out unsorted data over a specific protocol (GWT) [5]. The design of a fast, low power serializer was needed in order to reduce the power consumption in the front-end ASIC, which was one of the biggest design issues of the chip. Receiving time unsorted data over a different protocol forces the VELO sub detector group to a major redesign of the common readout board firmware, keeping untouched only the event building and the PCIe interface. VELO specific firmware developments are:

- Low Level Interface (LLI). It is the first layer of the firmware and it is responsible for the recovery of the data from the optical fibers, which is a customized and more extended version of the standard physical layer (PHY) in the OSI model. As the VELO Front-End ASIC uses its own protocol, a VELO LLI customize the Intel standard physical medium attachment and creates a new GWT physical coding sublayer.

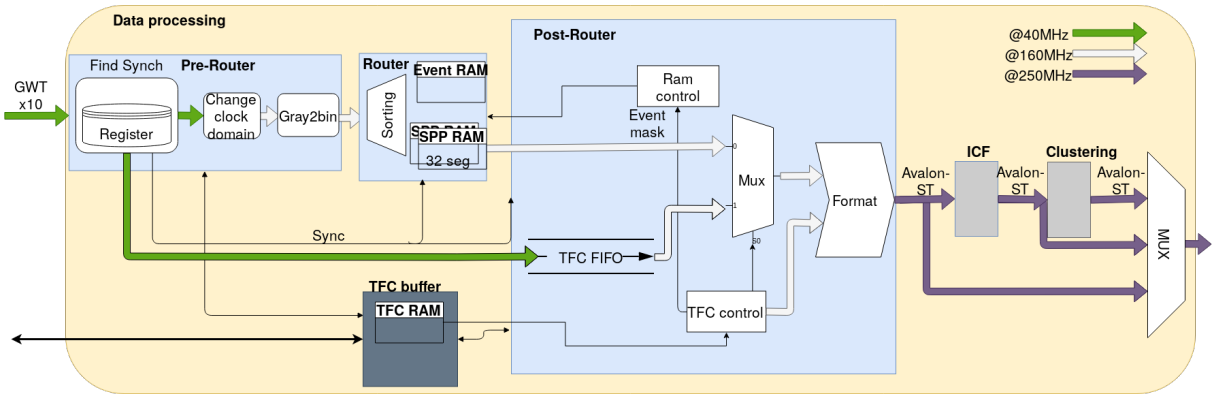

Figure 3: VELO back-end firmware processing scheme.

- Data Processing (Figure 3):
  - Pre-Router. Its main function is to trigger the data taking mechanism, change the clock domain from the 40 MHz of the LHC to the main data processing clock of 160 MHz, it also decodes the gray Bunch Crossing ID (BXID) from the VeloPix (VeloPix uses gray coded BXID in order to reduce the power consumption) and attach the ASIC ID.
  - Router. The main function of the back-end readout boards for VELO is performed in the Router and consists in sorting VeloPix data by its timestamp in real time and temporally store them in RAM memories. The main challenge of the router is the real time sorting of 10 GWT links without data loss and keeping reasonably low FPGA resources.
  - Post-Router. It reads the data from the Router RAMs, formats the data within the the LHCb common data format, encapsulate it in Intel Avalon streaming (Avalon-ST) protocol and fed it into the Event building block. It processes the TFC information associated to the back-end board and either discards or accepts the events.
  - Isolated Cluster Flagging (ICF). It searches for hit pixels and flag those surrounded by empty pixels. This flagging mechanism is intended for saving time in the software clustering and tracking algorithms performed in the CPU farm.
  - The implementation of, either partial or complete, real time cluster algorithm in the FPGA is under study with the same aim as the ICF. The design of the clustering is being made keeping a relatively small amount of FPGA resources to make it fit in the PCIe40 board.
  - The back-end board receives the timing information per bunch crossing from the read-out supervisor and stores it in a RAM memory (TFC RAM in Figure 3). VELO 's timing mechanism triggers the data acquisition when the Pre-Router receives a certain number of synch commands from the front-end, this information is propagated to the Post-Router where the core of the sync mechanism is implemented. The Post-Router sync mechanism reads the information per event from the TFC RAM starting from the sync bunch crossing and propagates the data according to the content of the RAM.

The minimum essential blocks for the VELO readout firmware are: Pre-Router, Router and Post-Router. The remaining blocks (ICF and clustering algorithm) will be implemented if enough FPGA resources are available. This configuration of the firmware requires around 75% of the FPGA memory blocks and 45% of the logic units. Once the clustering is included, the expected increase in FPGA resources is around 20% in logic resources and 5% in memory blocks. Extensive simulations have been done, showing that the minimum design option performs well within the specifications. Less than 10^{-6} of the crowdiest events in the readout board will be truncated in the firmware [6], those events will provide too many hits for track reconstruction and thus will be candidates for trigger rejection.

2.3 Bypass

A parallel design to the data acquisition firmware was developed with the aim of having a reliable way of acquire raw front-end data synchronously with the TimePix 3 telescope [7] (used as a reference) in a testbeam. Besides that, this firmware will be used in the VELO module production sites (University of Manchester and Nikhef) for quality assurance. This version of the firmware only shares with the final design the VELO LLI and the standard transceiver. The data processing's code is a completely new design. It triggers the reading mechanism of a link when a TFC sync command is received, packets the frame and stores it in an individual FIFO. FIFOs are read out through the PCIe interface giving priority to those with higher occupancies. In order to work in the test beam a synchronization mechanism was included. It takes the command that triggers the data acquisition and sent it out from an LVDS output to the Telescope.

3. Conclusion

The upgrade of LHCb VELO detector requires the design of specific firmware for controlling, synchronizing and reading the detector. In addition to the firmware used in the experiment, a testing and QA firmware was developed. This paper describes all varieties of VELO firmware.

References

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