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The upgraded readout electronics of the CMS ECAL: system overview

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The High Luminosity upgrade of the LHC at CERN will provide unprecedented instantaneous and integrated luminosities of around 5×10^{34} cm^{-2} s^{-1} and 3000 fb^{-1}, respectively, from 2025 to 2035. During this operational period, an average of 140 to 200 collisions per bunch-crossing (pile-up) is expected. In order to cope with these extreme pile-up conditions, increased data rates, and harsh environment, the Compact Muon Solenoid detector is undergoing a radical Phase II upgrade program. In the barrel region of the CMS electromagnetic calorimeter (ECAL) the entire readout and trigger electronics will be replaced. A dual gain trans-impedance amplifier and an ASIC providing two 160 MHz ADC channels, gain selection, and lossless data compression will be installed. The trigger decision will be moved off-detector and performed by powerful FPGAs, allowing for more sophisticated trigger algorithms to be applied.
The upgraded ECAL will be capable of high-precision timing measurements, of the order of 30 ps, for photons and electrons above 50 GeV. The time resolution improvement will enhance the overall CMS physics performance by mitigating the high pile-up effects.
The design of the full upgraded ECAL barrel readout chain and the status of the components R&D will be presented.

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1. Introduction

The High Luminosity LHC (HL-LHC) will provide a peak luminosity 5-7 times the nominal one and will deliver an integrated luminosity which will be about 10 times the expected luminosity of the first 12 years of LHC.

During HL-LHC, the CMS ECAL will have to cope with a challenging increase in the number of interactions per bunch crossing and higher radiation levels. The ECAL barrel (EB) on-detector and off-detector electronics have been completely redesigned to preserve detector performance with the goals of providing precision timing and low noise, allowing maximum flexibility and enhanced triggering possibilities. The primary driver of the EB upgrade are the CMS Level-1 trigger requirements: in particular a maximum latency of 12.5 μs and a Level-1 trigger rate up to 750 kHz compared to the current latency of 6.4 μs and trigger rate of 150 kHz. These requirements are both mandatory at HL-LHC in order to maintain the physics performance of CMS while exploiting the higher luminosity.

This paper will describe in Section 2 the ECAL barrel legacy readout architecture, in Section 3 the upgraded electronics for HL-LHC phase. A full description of the new Very Front-End (VFE) card, new Front-End (FE) card and the upgraded off-detector electronics will be given in Section 4 and 5 along with the status of the prototypes design and production.

2. The CMS ECAL Barrel readout architecture

The EB readout chain will maintain the present readout geometry of a 5 x 5 crystal matrix, the so-called trigger tower. Each lead-tungstate crystal is coupled to two avalanches photodiodes (APDs) and the signals are readout by a VFE card. Each VFE card receives signals coming from 5 crystals and the output of 5 VFEs are readout by a FE card and sent out to the off-detector electronics. The legacy readout system will not be able to satisfy the new requirements in terms of bandwidth and latency, so the on-detector and off-detector electronics will be replaced to meet these requirements.

3. The readout chain upgrade for HL-LHC

In the VFE board the Multi-Gain Pre-Amplifier (MGPA) will be replaced by the CATIA ASIC, a new custom chip, which will perform an enhanced discrimination between the anomalous APD signals[1] (spikes) and the correct ones [3]. The Multi-Channel ADC will be replaced by the LiTE-DTU ASIC which will sample the analogue signal at 160 MS/s, four times the sampling frequency of the legacy ADCs, with 12-bit of resolution. Moreover this ASIC will perform a sample selection and online lossless data compression. The CATIA and the high speed ADCs will improve the spike suppression capability of spikes and help to discriminate between energy deposits coming from different overlapping events.

In the upgraded FE card, the trigger primitive generation will be moved from the on-detector electronics to the back-end (BE) system. This shift will imply that the FE will not have to cope

[1]The anomalous APD signal is generated from direct hadron interaction in the APD, this signal is faster than the scintillation signal produced in the ECAL crystals, both in terms of arrival and signal rise time.

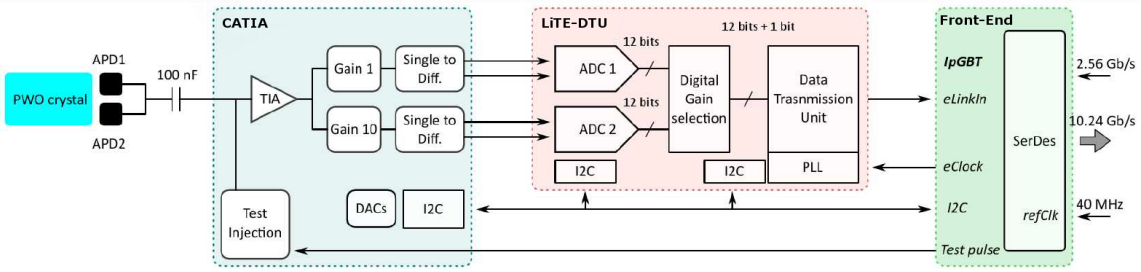


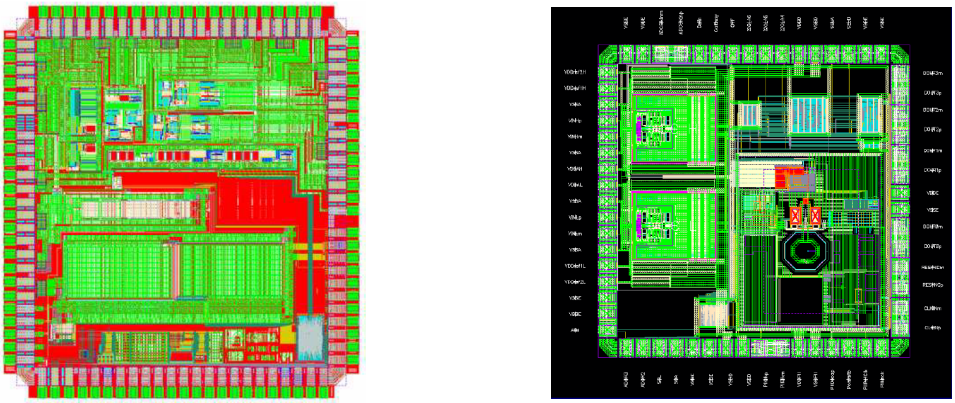
Figure 1: Schematic of the on-detector electronics upgrade. CATIA and LiTE-DTU ASICs will be hosted by the new VFE card which will be connected to the FE card through e-links.

with the Level-1 trigger constraints anymore. Fast rad-hard optical links will be employed in the FE card to stream all the single crystal data off-detector, as a result of this upgrade the trigger data granularity will have a 25 fold improvement.

4. Very Front-End ASICs: CATIA and LiTE-DTU

Two custom ASICs have been developed for the VFE upgrade: CATIA (CAlorimeter Trans-Impedance Amplifier), a fully analog ASIC designed in commercial CMOS 130 nm, and LiTE-DTU, a digital signal processing unit designed in commercial CMOS 65 nm technology.

The two ASICs will be hosted by a VFE board with the same form factor and cooling system as the legacy system. In Figure 2 are represented both CATIA and LiTE-DTU prototypes.



(a) (b)

Figure 2: (a) CATIA ASIC validator prototype and (b) first prototype of LiTE-DTU ASIC.

4.1 CATIA ASIC

The legacy readout chip (MGPA) hosted in the VFE and based on Charge Sensitive Amplifier (CSA) has been replaced by a high speed Trans-Impedance Amplifier (TIA), in order to follow as close as possible the input signal shape. The TIA will handle signals in a dynamic range from a few tens of MeV to 2 TeV equivalent electron/photon energies and the output dynamic has been splitted into two subranges by using two differential amplifiers with gain 10 and gain 1.

The first version of the CATIA ASIC has been submitted in 2016 [3], the main purpose of this demonstrator was the range optimization of the TIA. In 2018 the validator version has been submitted and then characterized with a laser light and connected to a commercial ADC. Moreover extensive beam test have been performed at CERN [4] using an electron beam with a momentum range between 25-250 GeV. The obtained results for the energy resolution measurements matched with the legacy electronics performance. Furthermore the time resolution on a single crystal measurement has shown that a 30 ps of time resolution can be achieved for an electromagnetic shower with an energy greater than 50 GeV. The final submission of the CATIA chip is foreseen for 2020.

4.2 LiTE-DTU ASIC

LiTE-DTU chip hosts 2 ADC IP block, a data selection, compression and transmission unit (DTU), an I^2C interface and a PLL for the high-speed clock generation, inherited from the Low Power Gigabit Transciever (lpGBT) chip. The ASIC has to tolerate a maximum total dose of 100 kGy and provide a single event upset protected control logic. The most demanding element of the LiTE-DTU is the ADC. For this reason, an external company has been involved in the design of the ADC IP block. The ADC has 12-bit of resolution, a sampling frequency of 160 MHz and a successive approximation architecture.

After the analog to digital conversion of the two CATIA output, the DTU selects, compress and serializes data. A look-ahead algorithm performs the sample selection between the two data streams with different gain. It consists of a continuous checking of the samples in order to trigger the presence of at least a saturated sample in gain 10 channel. When the trigger occurs, the algorithm allows the transmission of a slot of samples coming from the gain 1 channel. This saturation check is done in order to prevent the mixing of different gain samples in the same APD signal.

A lossless online data compression follows the gain selection stage, the former is executed in order to reduce the requested bandwidth for the data transmission and fit in the available one. A simplified Huffman encoding has been used [5], this compression code is based on the statistical distribution of the input values and assigns a variable length code to each input symbol inversely proportional to the symbol probability. During the compression, samples are packed in 32-bit words and thanks to this method the needed bandwidth for the data transmission is reduced from 2.08 Gb/s to 1.08 Gb/s [5]. Data packets are temporarily stored in a FIFO, which compensates the intrinsic rate packet variation due to the compression process[2]. IDLE words are transmitted in order to keep the serial link active and to avoid the loss of synchronization. Data packet from the LiTE-DTU are serialized to the FE board through differential electrical links at 1.28 Gb/s.

First LiTE-DTU prototype has been submitted at the end of 2018. The ADC characterization tests and the PLL clock qualification measurements are currently ongoing as well as the algorithms validation and the full ASIC radiation tolerance test.

5. Front-End board and Back-End electronics upgrade

The CMS ECAL Phase-2 FE has been designed to concentrate and stream all the data, generated on the VFE boards, to the CMS ECAL back-end electronics system based on the Barrel

[2]The samples are packed in two different data words: the first one takes 5 clock periods in order to be complete while the second type takes only 2 clock periods but it has a lower probability to occur [5].

Calorimeter Processor (BCP) ATCA modules [6].

The FE card will host 4 lpGBT ASICs with corresponding Versatile Link+ optical link modules. Moreover the new FE board will provide the clock distribution to the VFE boards and also manage the initialization and control signals of the VFE. As mentioned previously, the trigger primitive generation will be moved from the front-end to the upgraded off-detector system.

In the off-detector electronics upgrade, the BCP will host FPGAs and will receive data from the FE cards and to the Level-1 Trigger and DAQ system. The BCP board will receive the LHC clock and distribute it to the on-detector electronics, will handle the slow-control to the VFE-FE system. Moreover it will receive, decompress and serialize data and perform spike signal rejection. Lastly the BCP will send a set of pre-processed trigger primitive to the Level-1 trigger system and on the Level-1 accept signal the data to the DAQ.

6. Conclusions

The on-detector and off-detector electronics of he CMS barrel electromagnetic calorimeter will undergo an upgrade for the HL-LHC phase. The ECAL redout electronics will be replaced to cope with more demanding Phase-2 CMS trigger requirements, to maintain the best possible energy resolution, and to provide the needed much improved capabilities for pileup and spike suppression by means of precise timing measurements. Two custom ASICs have been designed for the upgraded VFE and a new FE board and off-detector electronics have been developed.
An important characteristic of the new readout architecture design will be the capability to provide precision timing measurements, of the order of 30 ps, for photons and electrons above 50 GeV. The excellent time resolution will improve the overall CMS physics performance by mitigating the high pile-up effects.

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