PROCEEDINGS OF SCIENCE

First lpGBT-based prototype of the End-of-Substructure (EoS) card for the ATLAS Strip Tracker Upgrade

Chaowaroj Wanotayaroj*[a], Artur Boebel[a], Harald Ceslik[a], Helmut Colbow[a], James Michael Keaveney[b], Mogens Dam[c], Sergio Diez[a], Peter Goettlicher[a], Jan Oechsle[c], Marcel Stanitzki[a], and Jonas Wolff[a]

[a] *Deutsches Elektronen-Synchrotron*
[b] *University of Cape Town*
[c] *University of Copenhagen*
E-mail: ma.x@cern.ch, artur.boebel@desy.de, harald.ceslik@desy.de, helmut.colbow@desy.de, james.keaveney@desy.de, dam@nbi.dk, sergio.diez.cornell@desy.de, peter.goettlicher@desy.de, jan.oechsle@cern.ch, marcel.stanitzki@desy.de, jonas.philipp.wolff@desy.de

The central building blocks of the ATLAS Strip Tracker Upgrade are the staves and petals which host up to 14 modules per side. The incoming data is sent to the EoS and multiplexed by the lpGBT chips on 10 Gbit/s links and sent via optical transmitters (VL+) off-detector. The EoS is a critical component for the upgrade, sitting at a single-point-of failure location. Prototype boards have been designed, manufactured and tested using the first available lpGBT and VL+ prototypes from CERN. We present the first test results and give an outlook towards the production of 2000 boards using these chips.

Topical Workshop on Electronics for Particle Physics TWEPP2019
2-6 September 2019
Santiago de Compostela - Spain

*Speaker.

PoS(TWEPP2019)114

1. Introduction and the role of the EoS

The silicon strip tracker for the ATLAS HL-LHC upgrade [1] consists of two geometries, each with its own geometrical planar substructures [2] holding the active modules: "Staves" for the barrel and "petals" for the endcaps. An End-of-Substructure card (EoS) is located at the far end from the interaction point. It will distribute the clock, control signal, and power to the modules and collect up to 28 data lines, each at 640 Mbits/s. The communication to off-detector is via optical links, one 2.5 Gbit/s down and up to two 10 Gbit/s links. The EoS is a single point of failure for large areas, therefore the EoS pair on both side of the plane is designed to be electrically separated and can work mostly independent of each other so that a broken EoS will only take down one side instead of the whole substructure.

2. The Design of the EoS

EoS-card hosts up to two serializers "low-powered Gigabit Transceivers (lpGBT)" [3] and a multichannel optical transceiver (VL+) [4], both are radiation-hard ASICs developed at CERN. Other passive components are for local power filtering, HV filtering and distribution, and signal conditioning.

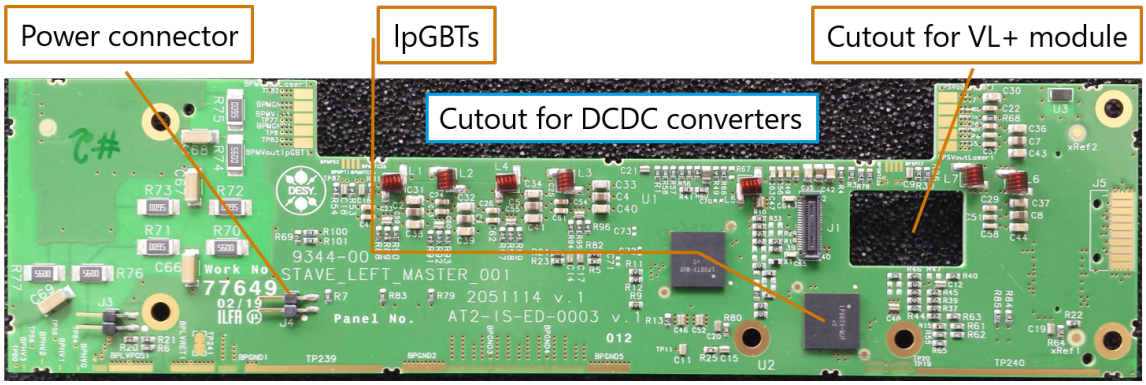


Figure 1: lpGBT based EoS Prototype. Shown here is an EoS card variant that hosts two lpGBTs.

The detector design and assembly restrict the total thickness of the EoS to be less than 5 mm. Building from our experiences with the prototypes with previous-generation active components [2], the lpGBT and VL+ based prototype is once again a twelve layers PCB with a nominal thickness of 1.6 mm and a 1.8 mm maximum, which is sufficient for high frequency power filters, impedance controlled signal distribution, and mechanical integration by gluing to a conductive support. Cutouts are included for the thicker components, as shown in Figure 1.

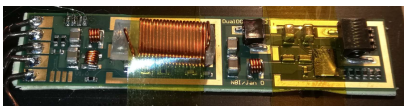


Figure 2: DCDC converters.

The smaller cutout provides more space for the VL+ module while minimizing the total thickness. The larger cutout is for DCDC converter modules (Figure 2) which are based closely on the CERN designs–the bPOL12V for 11 V $\rightarrow$ 2.5 V and bPOL2V5 for 2.5 V $\rightarrow$ 1.2 V. The coil and shielding box on top of the 1.6 mm EoS' PCB would violate the 5 mm limit. The power devices' fine structures with 0.3 mm ball-grid areas also demands higher heat transfer rate through the

PCB to the carbon fiber support structure which host the cooling pipes. Thus, the DCDC converters sit on a much thinner 0.2 mm PCB with just four layers.

The EoS cards have of a total of ten variants as a compromise between the functionality and mechanical constraints, and the manufacturing and quality control issues with lower production volumes. The variants are described in details in [2].

3. Test Setup and Results

Due to the limited and late availability of the newly designed lpGBT, only a few PCBs of one variant have been produced for the first tests. Moreover, the lpGBT will be configured as an I^2C slave instead of using register e-fuses to avoid permanent damage during the blowing process. This is due to the fact that the lpGBT blowing process in combination with the PCB design has not been verified yet. Since the DCDC converter will be tested separately, the 1.2 V and 2.5 V are supplied using a commercial DC power supply. Signals are probed or introduced by needles to test pads near the pads for later bonding to the substructures.

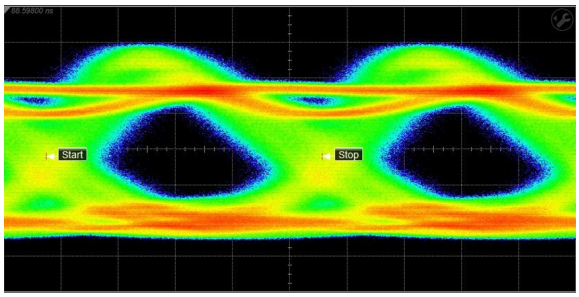
3.1 Test Firmware

Our test firmware are developed by incorporating lpGBT-FPGA IP cores from CERN [5]. It runs on Xilinx KC705 FPGA board, capable of reading and writing all ELinks on the EoS, as well as the lpGBT registers via the Internal Control (IC) field in the GBT protocol [3]. The firmware can perform a bit error rate (BER) test by sending bit patterns to the lpGBT and verifying the readout patterns on the other end. Since the roundtrip time-delay for the signal is unknown a priori, the firmware sends a fixed pattern and measures the shift before the actual test run.

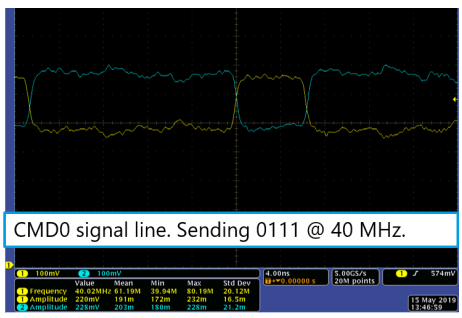
3.2 Functionality Tests

After checking a set of basic electrical properties for the PCB, we configured the lpGBTs and established the 10 G optical link. The first lpGBT is configured using an I^2C dongle connected to a PC. The second one however, has neither I^2C link to the outside or a downlink for the IC commands. Therefore, it is configured as a slave to one of the I^2C masters on the first lpGBT. The bunch-clock (40 MHz) is recovered from the optolink from the first lpGBT and transferred as electrical signal to the second lpGBT. This also demonstrates that the I^2C masters on the lpGBT works as expected.

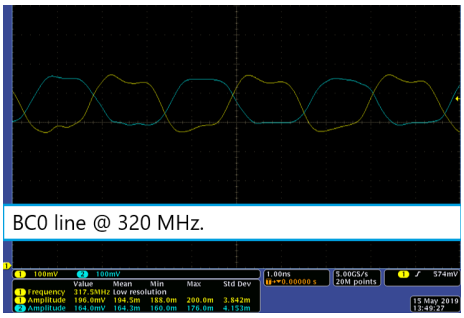
The eye diagrams for the 10 G link optical signal show open eyes, but with some jitter (Figure 3a). This is likely due to the fact that the clock was not directly recovered from the optical uplink data stream from the EoS because our device, the Keysight 86100D, cannot do that by itself. Instead, the downlink's reference clock was used. The E-link signal quality is tested for the TX-lines with a repetitive pattern of 0111 for easy inspection. The data rate of 160 Mbit/s is tested. Both show nice pulse shapes with rise time < 0.7 ns and only small overshoots. We plan to redo this measurement with better equipment and setup. This includes a custom design needle probe for E-link connections, clock recovery from data stream (the clock recovery unit Keysight N1077A will be used for future tests), and with the DCDC converter prototype before finalizing our EoS designs.



(a) 10 G eye diagrams



(b) Elink Tx: 0111 at 160 Mbit/s



(c) 320 MHz clock from the EoS

Figure 3: Output signals from the EoS.

3.3 Bit Error Rate (BER) Test

Preliminary BER tests with an ad-hoc setup (e.g. the connection to the EoS E-link is a needle touching the bond pads.) have been done for both uplink and downlink, and both lpGBTs in a two-lpGBTs EOS for ∼6 hours. First the Forward Error Correction (FEC) information is used to verify the packet, and only if it indicates no bit error then the bits will be compared. If FEC found an error, we count the whole package as error to get the estimate of the worse case scenario because we want to learn about the error due to our hardware design. The result are shown in Table 1. This does not satisfy our $< 10^{-12}$ requirements, but there are several possible improvements. The setup is an ad-hoc as mentioned. Also, the reference clock used does not pass the jitter requirements recommended by the lpGBT designer. They suggest an external 320 MHz low-jitter clock for the FPGA's transceiver, but this is impractical for testing 2000+ boards. Instead, a 160 MHz clock generated on the FPGA board is used. A comparison with a test using external clock is already planned.

4. Conclusion

We successfully built lpGBT and VL+ based EoS prototypes that met the constraints from detector design, as well as an accompanying test system. Functionality and BER test results, with limited statistics, showed that our prototypes work with a few exceptions where the results fall below the requirements. They are under investigation and we expect it to be improved with better equipment in the future production.

lpGBT	Direction	Error Type	#Error	BER
#1	Uplink	FEC	0	0
#1	Uplink	Bit	2	1.45×10^{-13}
#2	Uplink	FEC	432	1.95×10^{-12}
#2	Uplink	Bit	8	5.79×10^{-13}
#1	Downlink	Bit	0	0

Table 1: The bit error rate test results. The BER numbers count a FEC error as one bit error.

Acknowledgement

We would like to acknowledge the Helmholtz Association HGF, and DST/NRF, South Africa for the support.

References

[1] ATLAS Collaboration, "Technical Design Report for the ATLAS Inner Tracker Strip Detector," CERN-LHCC-2017-005, ATLAS-TDR-025.

[2] C. Wanotayaroj, et al., "The End-of-Substructure (EoS) card for the Strip Tracker Upgrade of the ATLAS experiment," https://doi.org/10.22323/1.343.0130.

[3] The GBT Project, "lpGBT Manual," https://lpgbt.web.cern.ch/lpgbt/manual/.

[4] VL+ Team, "Versatile Link Plus Transceiver," https://espace.cern.ch/project-Versatile-Link-Plus.

[5] The GBT Project, "GBT-FPGA," http://gbt-fpga.web.cern.ch/.