PROCEEDINGS OF SCIENCE

The OBDT board: a prototype for the Phase 2 Drift Tubes on-detector electronics.

Javier Sastre Álvaro
Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas.
Av. Complutense, 40, 28040 Madrid - Spain
E-mail: javier.sastre@ciemat.es

Andrea Triossi
Institut Pluridisciplinaire Hubert CURIEN.
23 rue du loess - BP28, 67200 Strasbourg - France
E-mail: andrea.triossi@iphc.cnrs.fr

Antonio Bergnoli
INFN Sezione di Padova; Università di Padova.
Via 8 Febbraio, 2, 35122, Padova, Veneto, Italy
E-mail: antonio.bergnoli@cern.ch

Alessandro Griggio
INFN Sezione di Padova; Università di Padova.
Via 8 Febbraio, 2, 35122, Padova, Veneto, Italy
E-mail: alessandro.griggio@cern.ch

David Redondo Ferrero
Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas.
Av. Complutense, 40, 28040 Madrid - Spain
E-mail: DavidDaniel.Redondo@ciemat.es

On behalf of the CMS muon group.

We present here the design and performance of the On-Board electronics for Drift Tubes board (OBDT), which is the new prototype built to substitute the Drift Tubes (DT) muon on-detector electronics at Compact Muon Solenoid experiment (CMS). The OBDT is responsible of the time digitization of the DT signals, allowing further tracking and triggering of the barrel muons. It is also in charge of the slow control tasks of the DT chamber systems. A prototype of this board has been produced and is being tested both in the laboratory and also in test stands with real DT chambers. The full functionality in real conditions is being evaluated, showing very satisfactory results.

Topical Workshop on Electronics for Particle Physics (TWEPP2019)
2-6 September 2019
Santiago de Compostela, Spain

PoS(TWEPP2019)115

1. Overview

The Drift Tubes (DT) detector [1] is in charge of muon identification, reconstruction and triggering in the central region of CMS. The present electronics, the Read Out Boards (ROB), perform the time digitization of signals generated by the DT and the selection of valid hits on reception of a Level 1 Accept (L1A) trigger signal. These ROBs, together with all the on detector electronics for DTs, will need to be replaced for HL-LHC in order to accommodate to the new conditions, among others, the increase in L1A rate beyond the maximum 300 kHz that ROBs will withstand [2]. The new electronics needs a time resolution of 1 ns on at least 240 channels per board, very good linearity and needs to be capable of operating with hit input rates of up to 2 MHz and L1A trigger rates of up to 1 MHz.

2. The OBDT board for DTs at HL-LHC

The OBDT (On detector Board for Drift Tubes) is the new board that is being designed to substitute the ROB electronics for HL-LHC. It will perform the time digitization of the incoming signals and will forward all the received information up to the backend electronics, which will be in charge of performing not only the readout but also the trigger primitive generation of the DT chambers to be forwarded to the central muon Trigger system. In addition, the OBDT board needs to perform other tasks such as the slow control of legacy electronics.

The complexity of the on detector system will be reduced from 14 boards per chamber to 5 in the worst case, reducing power consumption by approximately 60%.

3. OBDT board description

The OBDT board is built using a Microsemi Polarfire MPF300 FPGA. The time digitization of up to 240 channels is performed inside this FPGA through a deserialization method. Each input signal is sampled by a 600 MHz DDR deserializer, and then 0 to 1 transitions are detected in the parallel array of sampled data. The detected transitions are converted to a digital value which includes the coarse count in steps of the LHC bunch crossing (BX), that is 25 ns, and a fine bin size with a least significant bin of 1/30 of a BX. That is, the least significant bin of the TDC (Time to Digital Converter) is 0.833 ns.

As can be seen in figure 1, the slow control and synchronization of the OBDT is made through the GBTx chipset [3]. An SFP+ transceiver and bidirectional optical link allow forwarding not only the monitoring and configuration information but also and most importantly, the timing information from the LHC, such as the 40.076 MHz clock and the Bunch Counter reset signals (and other synchronization signals). The GBT ASIC receives this bit stream, forwards the clock to the FPGA and also allows communication to the FPGA and to the SCA ASIC through e-link channels.

Among other functionalities, the SCA allows the generation of the voltages for threshold, bias and width that are required for the proper configuration of the Front End Boards (FEB) that discriminate the input signals. Also, it allows measuring the voltages in the different parts of the electronics and the temperatures. The SCA also includes several I^2C links for communication with legacy electronics.

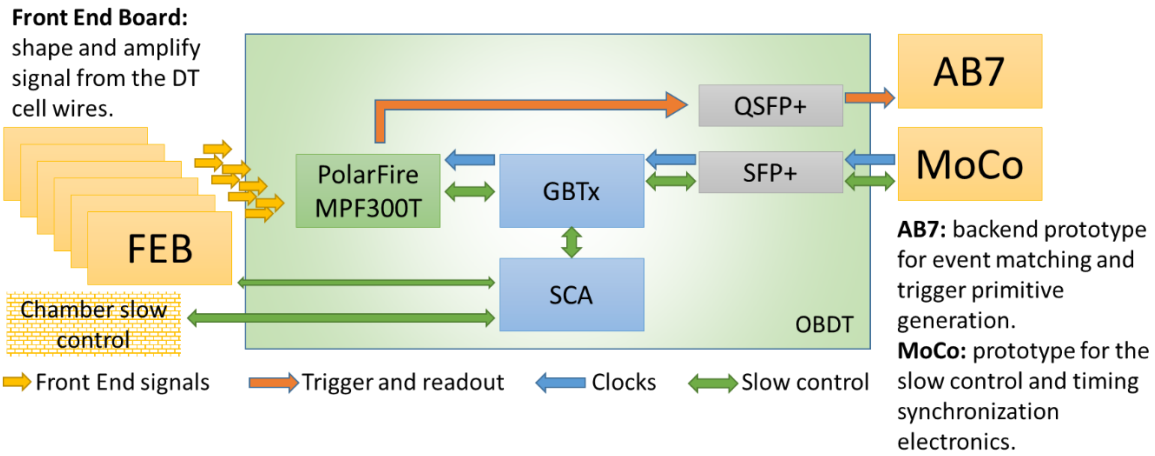

Figure 1: Diagram of the OBDT main functional blocks.

The SCA chip also allows setting the currents that are needed for injection of the Test Pulse (TP) signals for DT chambers calibration.

Once the input hits are received by the Polarfire FPGA, the digital information is merged through a serializer and forwarded to the trigger backend. Data is formatted as a GBT protocol frame and sent through a serial high speed link using a QSFP optical transceiver, providing an output bandwidth of 3.36 Gbps.

In figure 2, the different firmware blocks of Polarfire FPGA can be seen. Input hits are received from the FEB lines. A reference clock is received from a dedicated port of GBTx, which also sends a faster clock (320 MHz) and slow control information to the FPGA through the e-link lines. On the other hand, the FPGA outputs Testpulse signal to the FEB and the output data that is sent formatted in a GBT protocol to the next level of the electronics chain to AB7. It is to be noted that the synchronization commands from the Timing and Control Distribution System (TCDS) system such as Bunch Crossing 0 (BC0) and Orbit reset (OC0) are received from the e-link protocol and decoded in the Timing and Trigger Control (TTC) block.

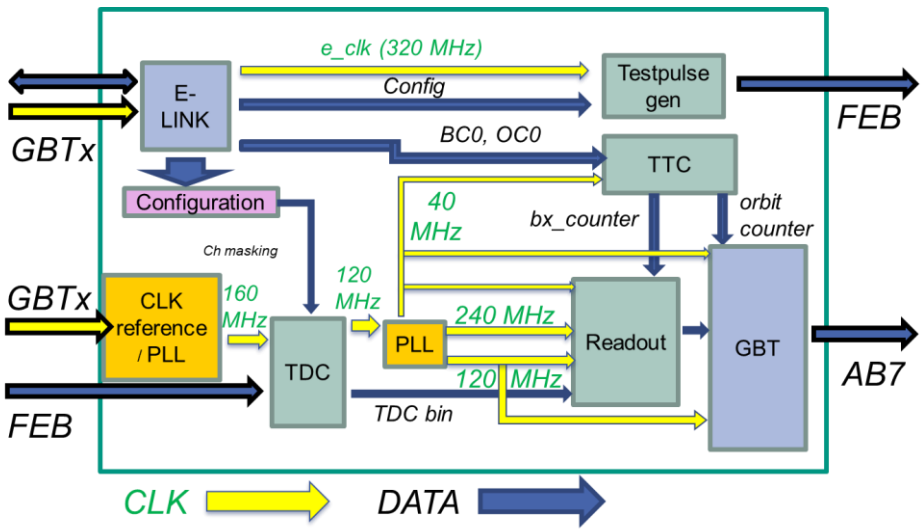

Figure 2: Diagram of the Polarfire FPGA firmware blocks of the OBDT board.

4. Validation of the OBDT

Several validation tests have been performed with OBDT prototypes. The first ones correspond to the measurements of the timing performance and, in particular, the Differential Non Linearity (DNL) of the different input channels, which were performed by injecting a non-correlated random signal. The results can be seen in Figure 3 and they show that the DNLs are within the requirements of +-10% and that there are some differences which seem to correspond mainly to the different blocks of time digitization instantiated in the FPGA. Measurements of channels crosstalk have also been performed and they are shown in Figure 4 (*left)*, where the DNL of one channel was measured with and without a neighboring channel having a signal injected. As can be seen, the effect of the neighboring signal is visible but it is below 1%.

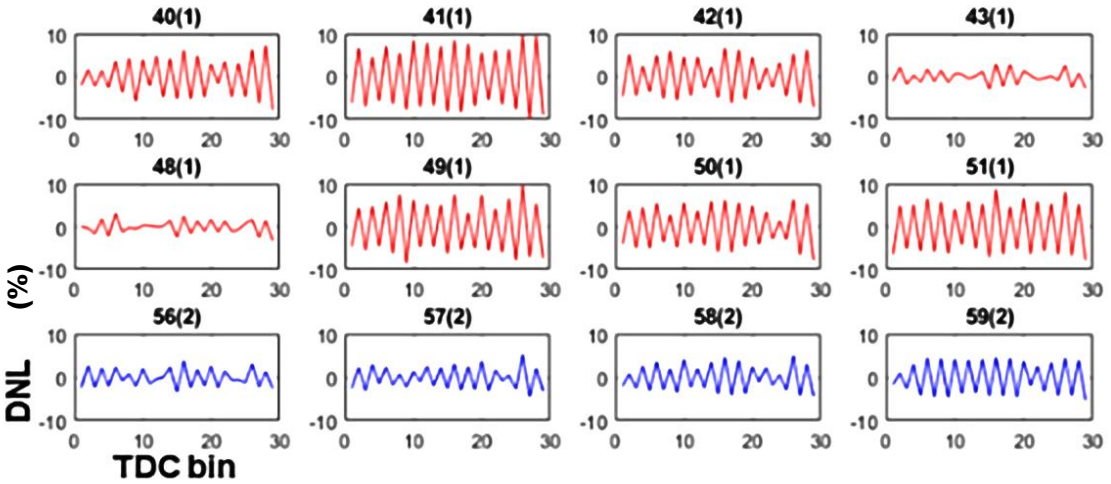

Figure 3: Images of some DNL measurements performed in different channels of the OBDT board.

Other critical tests performed are related to the power consumption and the efficient cooling of the board in the final location in CMS, embedded into the wheels where only cooling through water conduction at 17ºC is possible. Temperature remains low and stable as shown in Figure 4 (*right*). With a total power consumption of 16 W, the OBDT can be cooled down effectively and the temperature remained stable for more than an hour.

Finally, the OBDTs were installed in the CMS detector as part of a data taking campaign called Slice Test and which intended to validate the HL-LHC electronics connected to the DT chambers with the expected power supplies distribution and integrated in the Timing, Trigger, DAQ and slow control systems of CMS. The full chain is operational and data taking is happening satisfactorily. Tests included cosmic and test pulses runs.

In Figure 5, the timebox distribution of the hits from DT cells is shown, with the occupancy of each of the chamber cells and the timeboxes, which represent the time distribution of the hits generated in the 400 ns drift time of the cells.

5. Summary

The first prototype of the OBDT board contains all the required functionality and has passed all qualification tests. Radiation tolerant tests are expected soon. These boards have been installed in the CMS detector in a parallel Slice Test with the legacy electronics. The new cards are part of

regular cosmic ray data taking and are fully integrated into CMS. First results indicate that the OBDT cards can successfully perform the time digitization and the slow control tasks required.

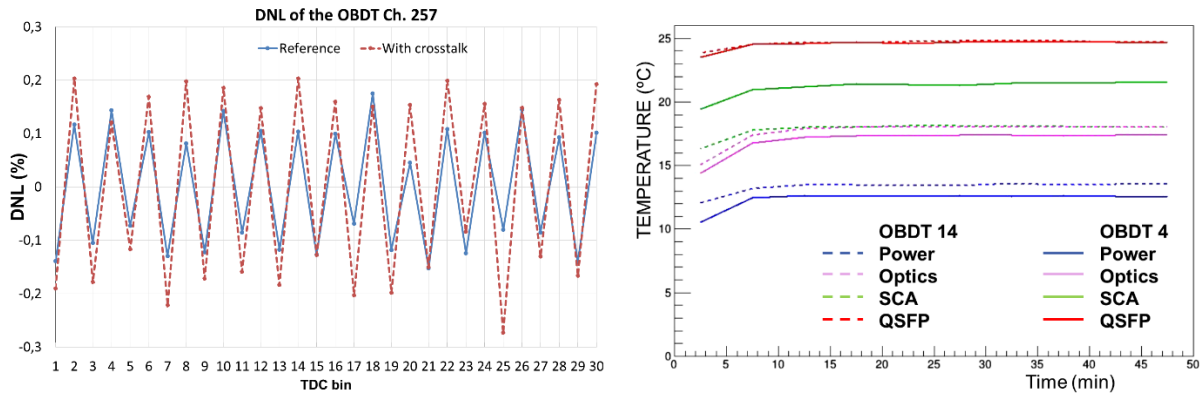

Figure 4: (*left*) Differential Non Linearity of channel 257 of the OBDT board with and without crosstalk from a neighboring channel. (*right)* Image of the temperature stabilization of the different sensors of the OBDT when performing cooling tests installed in the mechanical frame.

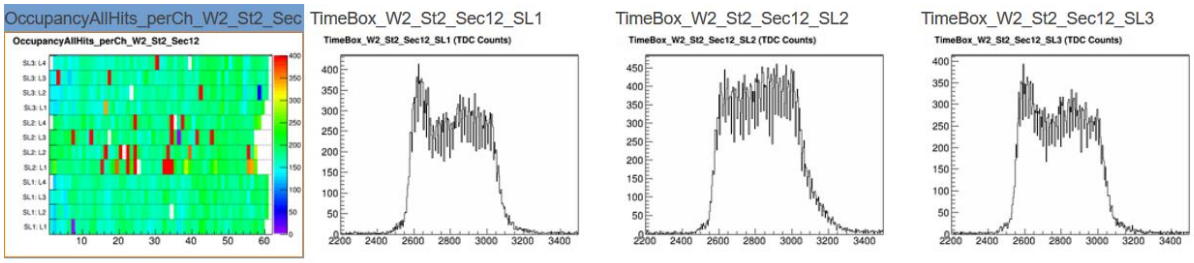

Figure 5: Image of the Data Quality Monitoring display from CMS with the information recorded by the OBDT electronics in a cosmic ray data taking campaign.

References

[1] CMS Collaboration. "The Muon Project Tech. Design Rep", CERN/LHCC 97-32, Dec. 1997.

[2] CMS Collaboration. "The Phase-2 Upgrade of the CMS Muon Detectors." CERN-LHCC-2017-012; CMS-TDR-016. September, 2017.

[3] P. Moreira. "The GBT, a proposed architecture for Multi-Gb/s Data transmission in High Energy Physics." Proceedings of the Topical Workshop on Electronics for Particle Physics. September 3-7, 2007. Prague, Czech Republic.