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Module and System Test Development for the Phase-II ATLAS ITk Pixel Upgrade

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In the high-luminosity era of the Large Hadron Collider, the instantaneous luminosity is expected to reach unprecedented values, resulting in up to 200 proton-proton interactions in a typical bunch crossing. To cope with the resulting increase in occupancy, bandwidth and radiation damage, the ATLAS Inner Detector will be replaced by an all-silicon system, the Inner Tracker (ITk). The innermost part of the ITk will consist of a pixel detector, with an active area of about $13\,\mathrm{m}^2$. In order to cope with the changing requirements in terms of radiation hardness, power dissipation and production yield, several different silicon sensor technologies will be employed in the five barrel and endcap layers. With the arrival of the first readout chip prototype, the RD53A chip, the development of hybrid detector modules is starting to address numerous production issues, understanding of which will be crucial for the layout and production of the final ITk pixel detector modules. In addition, the new powering scheme is serial which gives further challenges. A large prototyping programme on system test level is ongoing. Components for larger structures with multiple modules based on the FE-I4 front-end chips were produced and are under evaluation. This contribution presents the latest development from the assembly and characterisation of prototype modules as well as the latest evaluation and results of fully electrical prototypes.

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1. Introduction

With the High-Luminosity Large Hadron Collider (HL-LHC) starting around 2026, the number of proton-proton collisions per bunch crossing increases from 30 to 200 on average. To cope with the resulting increase in occupancy, bandwidth and radiation damage, the ATLAS [1] Inner Detector (ID) will be replaced by an all-silicon system, the Inner Tracker (ITk), as its Phase-II upgrade. A finer granularity, faster signal processing and data transmission are required to maintain the occupancy to below 1 % and handle a higher trigger rate of 1 MHz, while the innermost layer has to withstand up to $2 \cdot 10^{16}$ 1 MeV $\mathrm{n_{eq}/cm^2}$.

Compared to the current ID the surface area of the ITk pixel system increases from 1.7 $\mathrm{m^2}$ to 13 $\mathrm{m^2}$, resulting in $5 \cdot 10^9$ readout channels. Figure 1 (a) shows the comparison between the current pixel detector and the ITk Pixel. The 5-layer module layout of the ITk Pixel, as shown in Figure 1 (b), is divided into three subsystems: the Inner System including services (not shown) up to $r = 139$ mm, the Outer Barrel that extends to $z = 1110$ mm, and the Outer Endcap.

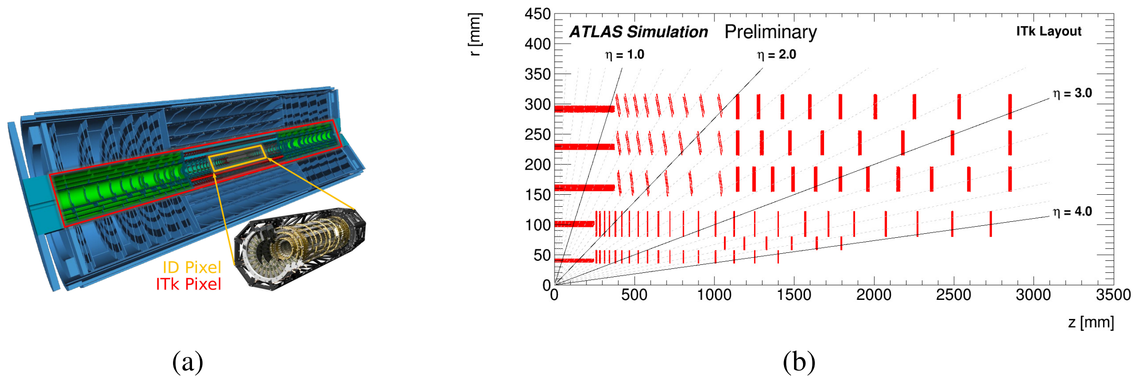

Figure 1: (a) Comparison of the ID[1] and ITk [2] in size and layout. The blue shows the ITk Strip and the green shows the ITk Pixel. (b) The ITk Pixel module layout [3].

2. ITk Pixel Module and System Tests

In the Inner System and Outer Endcap the modules are attached onto carbon composite staves with adhesives while in the Outer Barrel the modules are loaded onto thermal pyrolytic graphite heat spreaders on aluminium-graphite cells before being screwed onto a stave.

Figure 2 shows the components of a quad module. Each module is made of a flexible PCB onto which a sensor, bump-bonded onto four FE chips, is glued. The electrical connection for reading out the FE chips is done with wirebonds onto the flex. The backside of the FE chips are glued onto local support.

2.1 Sensors

The ITk sensors are required to have a hit efficiency at orthogonal particle incidence of >98.5 % before and >97 % after irradiation. Two different sensor technologies will be used: 3D sensors in

[1] https://cds.cern.ch/record/1095925

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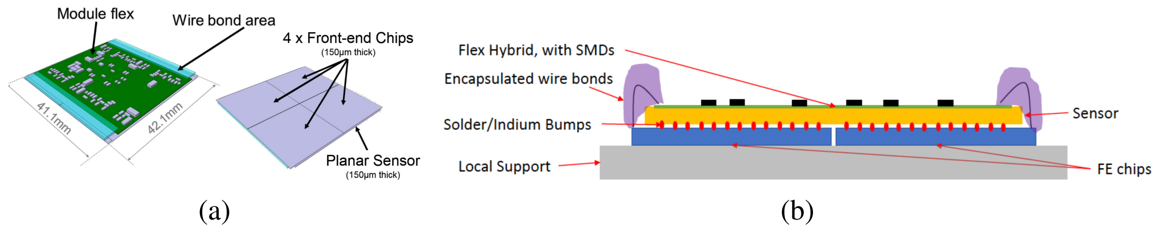

Figure 2: (a) Overview of a quad module and its components. (b) Cross-section of the module stack-up.

layer 0 for the better radiation tolerance, and planar sensors in layers 1–4. The planar sensors have a pixel size of $50 \times 50\,\mu\text{m}^2$, while for 3D sensors $50 \times 50\,\mu\text{m}^2$ and $25 \times 100\,\mu\text{m}^2$ are under evaluation.

2.2 Frontend Chip and Flex PCBs

The readout chip is developed by the RD53 collaboration [4]. The first prototype FE chip, RD53A [5], is half the final size with 400×192 pixels of $50 \times 50\,\mu\text{m}^2$ size distributed over $11.6 \times 20\,\text{mm}^2$. It is capable of handling a hit rate of $3\,\text{GHz/cm}^2$ compared to the current readout chip FE-I4 with $400\,\text{MHz/cm}^2$ [6]. Data are transferred via 4 lanes with 1.28 Gbit/s each. This 65 nm technology is tested to work up to 500 Mrad total ionising dose. The full-size production chip, ITkPix-V1, is being prepared for submission.

RD53A chips can be powered in shunt-LDO [7] mode that provides a constant current, which is essential for a stable serial powering operation. More than 250 chips have been successfully tested on single chip cards. The tests include automated wafer probing, tuning of unirradiated and irradiated modules, irradiation of chips with X-ray and radioactive sources, testbeams and serial powering [8].

Flexible PCBs have been designed for the programme with RD53A modules. Digital modules have been built for the design verification of the quad and triplet PCBs that are shown in Figure 3 (a) and (b). Figure 3 (c) shows a single module with a red rectangle outlining the position of the RD53A chip and thus the active area. It responds as expected to a source scan, as can be seen in the occupancy map in Figure 3 (d). The parts with lower number of hits correspond to the SMD components on the module PCB, the higher occupancy in the top right corner is due to the opening in the PCB for the HV wirebonds.

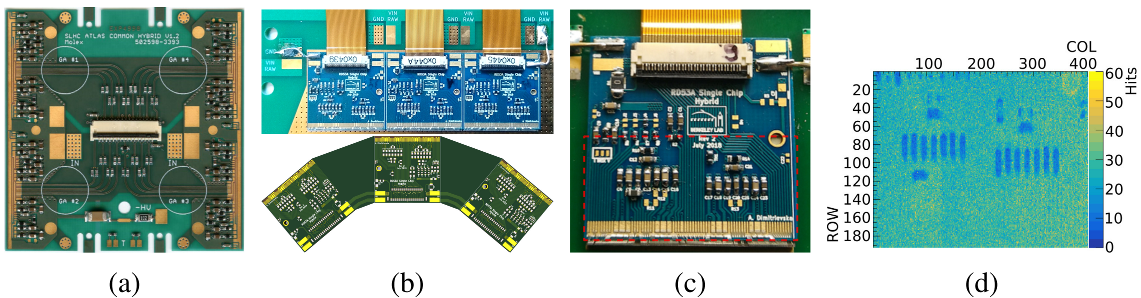

Figure 3: (a) A quad module PCB. (b) A triplet module for the barrel section (top) and a triplet PCB for the ring section (bottom) of the Inner System. (c) A single module on a PCB, where the red rectangle outlines the RD53A chip. (d) An occupancy map from a source scan on the active area of a single module.

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2.3 High-Voltage and Wirebond Protection

Irradiated sensors require higher bias voltage of up to 600 V for the ITk planar sensors. This large potential difference between sensor and FE chip can cause discharge near the module corner as shown in Figure 4 (a), which can be reduced by electrically insulating the FE and sensor via benzocyclobutene (BCB), polyimide or Parylene coating.

A BCB or polyimide coating of 3 μm thickness can be applied during wafer processing, thus cannot protect the dicing edge and requires an additional step in photolithography to open bump-bond pads. Only a few BCB coated samples have been tested where discharge was observed at voltages below 800 V.

Parylene coating of 5–7 μm thickness is applied after module assembly and wirebonding and thus can coat the module (with cell) as a whole, whereas electrical and thermal contacts have to be masked. 41 modules have been successfully tested to over 800 V.

To avoid exposure of wirebonds to damage, materials for encapsulation, as shown in Figure 4 (b), are being studied, e.g. silicones, urethanes, low CTE epoxies and conformal coating with Parylene. Thermal cycling can potentially break wirebonds and bump bonds due to thermal stress. Irradiation can harden the material, make it brittle and induce cracks or peel-off. Thick parylene coating of up to $\sim$50 μm can provide some mechanical protection and can be reasonably radiation hard. Studies on thermal cycling, irradiation and the combination thereof are ongoing for different encapsulants.

Noise as one of the indicators of the performance is measured at each production stage of a module. Figure 4 (c) shows noise measurements of a quad FE-I4 module after four production stages: bare module and PCB assembly (assembled), wirebond encapsulation (encapsulated), both measured at approximately 0°C on the module PCB. The measurements after loading onto local support (on local support) and bending of the power and data pigtail (bent) were conducted in a different setup with 17°C measured on the module PCB. The variation in noise between each step is small and well within the uncertainties.

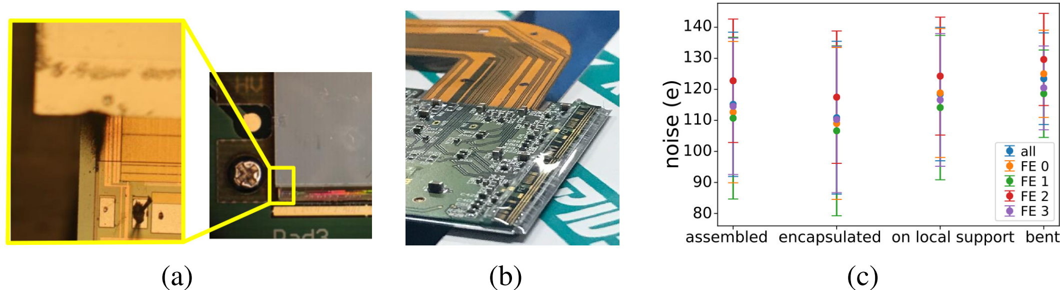

Figure 4: (a) Close-up of a module edge where spark occured. (b) An FE-I4 quad module with encapsulated wirebonds. (c) The noise level of a quad FE-I4 module after different production stages.

3. System Tests with FE-I4 Modules

Until RD53A modules become available, system tests are already ongoing with modules based on FE-I4 chips, which are loaded onto demonstrator staves to test and validate the aspects of a

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fully integrated system. The demonstrators reside in interlocked testboxes with e.g. CO_2 cooling, realistic services, power supply units and control systems. Figure 5 shows the partially loaded Outer Barrel demonstrator in (a), which is fully functional and can be powered in several serial chains [9]. Figure 5 (b) shows a source scan of the flat section of the Outer Barrel demonstrator, obtained using a Sr90 source mounted on a linear stage. The number of hits is indicated by the colour scale. Patches and patterns with lower number of hits are expected and correspond to the SMD components on the module PCB and the bent pigtail over the modules. Higher average number of hits on the three central modules are due to a different kind of PCB, while in the far right module the pigtail region has a much lower occupancy that is due to a higher copper thickness compared to the other modules. During the assembly and loading process, modules are tested and compared after each step to check for any potential degradation in performance. A second prototype, assembled for the endcaps, was also tested in detail. Results of the noise measurements of the modules before and after loading onto the endcap stave is shown in Figure 5 (c) by the blue and red crosses, respectively. The change is negligible compared to the uncertainties and the variation between different modules.

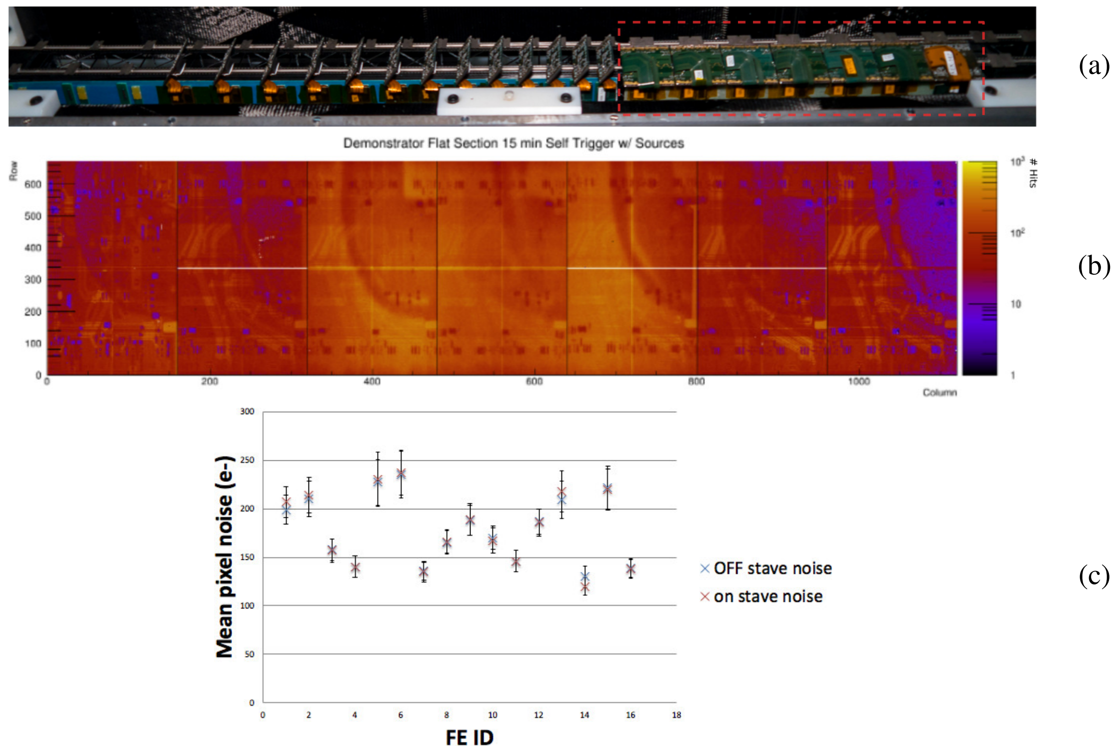

Figure 5: (a) Full-length Outer Barrel demonstrator partially loaded with dual and quad modules. The flat section in the red rectangle is where the source scan in (b) is performed on. (c) Comparison of module noise before and after loading onto an endcap stave.

4. Conclusion

The components for the ATLAS ITk Pixel modules are being characterised and improved. Experience on assembly and procedures have been gained with FE-I4 prototypes, which are im-

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plemented into diverse demonstrators. Large scale demonstrators of each subsystem are getting ready for RD53A modules, which are currently being produced and foreseen for next year, to be evaluated in aspects of system and serial powering tests.

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