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Design of a 4 ps radiation hardened TDC with an improved interpolation technique

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This paper presents a radiation tolerant single-shot time-to-digital converter (TDC) with a resolution of 4 ps, fabricated in a 65 nm Complementary Metal Oxide Semiconductor (CMOS) technology. To achieve the low resolution, the delay elements are implemented using a new interlocked interpolation technique to reduce the Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) error. The delay line is placed inside a Delay Locked Look (DLL) to compensate for Process, Voltage and Temperature (PVT) variations- and variations due to ionizing radiation.

Topical Workshop on Electronics for Particle Physics TWEPP2019
2-6 September 2019
Santiago de Compostela - Spain

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PoS(TWEPP2019)127

1. Introduction

TDCs can be compared to Analog-to-Digital Converters (ADCs) as they digitize analog-like time differences instead of analog voltage differences. Several applications require precise time measurements such as particle tracking in high energy physics [1], where a high resolution TDC is required to distinguish tracks from different vertices. Also inside Time-Of-Flight distance measurements [2] and many other circuits like frequency synthesizers, clock generators, clock data recovery circuits (CDRs)[3], time-domain ADCs [4] and jitter measurement circuits [5], the on-board TDC is critical to the overall performance of the circuit. High-performance TDCs thus require a small quantization delay, low noise, large sampling speed and high linearity. One of the main challenges for increasing the resolution of the TDC, is overcoming the minimum gate- delay of the technology. The methods which are commonly used to overcome this problem are, the Vernier architecture [6], (passive or active) interpolation [7] and the parallel TDC [8]. All of these architectures come with their own challenges, but the most suitable architecture for the mentioned applications is the passive interpolation because the interpolation resistors do not suffer from TID (Total Ionising Dose).

In this design an improved form of passive interpolation is proposed, which aims to reduce the non-linearity error compared to the known technique. This paper is structured as follows: in section 2, the architecture of the TDC is described, in section 3, the novel interpolation technique is discussed followed by the simulation results which are based on parasitic extracted models to reflect the phyisical chip as much as possible.

2. Architecture Overview

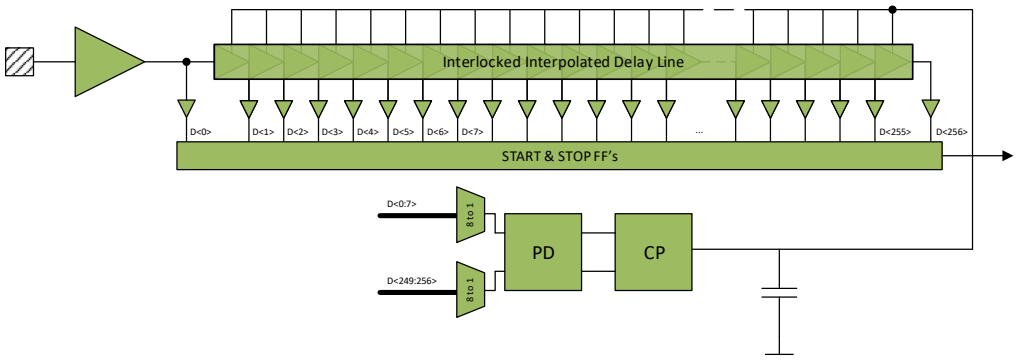

Figure 1: Architecture of the Time to Digital converter.

The quantisation of the input time difference is achieved by sampling a time reference on the start of the event and on the end of the event. The difference is then taken between these two measurements which results in the quantised duration of the event. The timing reference used in this architecture (Figure 1) is a delay-line consisting of 64 chained pseudo differential delay elements, which work as a tunable buffer. To stabelize the total delay of the delay-line to a fixed delay, it is placed inside a DLL (Delay Locked Loop). This loop structure fixes the delay of the delay-line to the period of an input reference clock, using a PD (Phase Detector), CP (Charge Pump) and LF (Loop Filter). With this loop, possible PVT (Process, Voltage and Temperature)

variations and variations due to TID are compensated [9]. The PD used in this architecture is the same coming from a previous design [10]. This bang-bang style PD uses an extra reset state in-between the phase detector states to reduce the hysteresis, which results in a smaller output jitter of the DLL. The charge pump in this architecture can be adjusted to tune the BW (bandwidth) of the DLL, for achieving the best possible output jitter of the DLL. The DLL is a first order system which is intrinsically stable. the loop filter also only consists of a regular MoM (Metal on Metal) capacitor.

To sample the DLL, two sample registers consisting of standard D-Flip Flops are used. These registers can independently be sampled by a start and a stop trigger respectively. A digital decoder converts the raw DLL code from the registers and takes the difference from both samples. This will output the quantised duration time of the measured event, represented in a binary output value. This value can be used for further digital processing.

3. Interpolation Technique

To overcome the minimum gate-delay of the technology, the passive interpolation technique is used. this technique involves to connect a chain of resistors around the individual delay elements from input to the output. the amount of resistors determines the interpolation number and the divider of the gate-delay of the buffer. In this design the delay elements in the delay line are interpolated four times, which reduces the gate-delay also four times. It can be seen that by increasing the interpolation number, the gate-delay can be decreased even further. Nevertheless, the minimal gate-delay, when using passive interpolation is still determined by the non-linearity error of the delay buffer. Furthermore, to make the interpolated bin size equal across the delay element it is not as simple as using equal resistors, because every interpolation node is loaded with the subsequent interpolation resistor. This makes it harder to determine the correct value of the interpolation resistor, which is especially the case for interpolations beyond four times. Currently the resistors are tuned based on parasitic extracted models from the layout design in an iterative way.

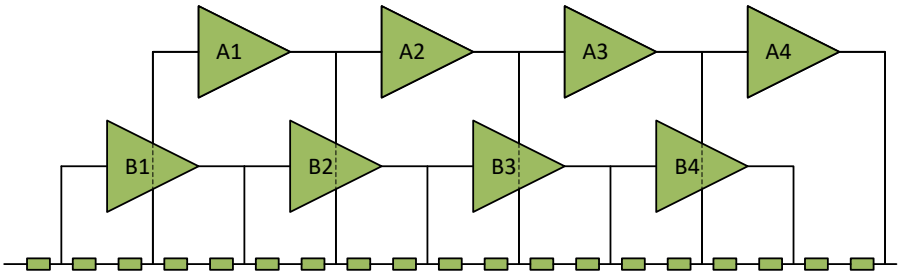

Figure 2: Interlocked interpolation technique using two parallel delay lines interlocked every two interpolation resistors.

In this design a novel technique for passive interpolation is proposed. As shown in Figure 2 the interpolation is accomplished using two separate delay lines which are interpolated four times but interlocked every two resistors. First, this improves the DNL (differential non linearity) error because, every two nodes will be driven by a delay buffer which makes the influence of the loading of the next state have a smaller impact. Second, the need for fine tuned resistors is gone because

now every two nodes the net is driven. This means equal resistors can be used which makes the layout design more lithografic friendly and improve the mismatch. Third, the overall Non-linearity error decreases because the driving power of the delay line doubled because of the two delay lines connected together.

4. simulation results

To compare the novel design technique of the passive interpolation, simulations are performed comparing the interlocked interpolation against two regular interpolations. The resistive interpolation across the three simulations is the same and all resistors have the same value. Figure 3 shows the DNL and INL error of the three simulations. It can be seen that the repetitive error due to the resistive interpolation occurs in all simulations. Nevertheless in the interlocked interpolation (blue) the peak to peak error is 2.4 times smaller compared to the regular interpolation (red,yellow).

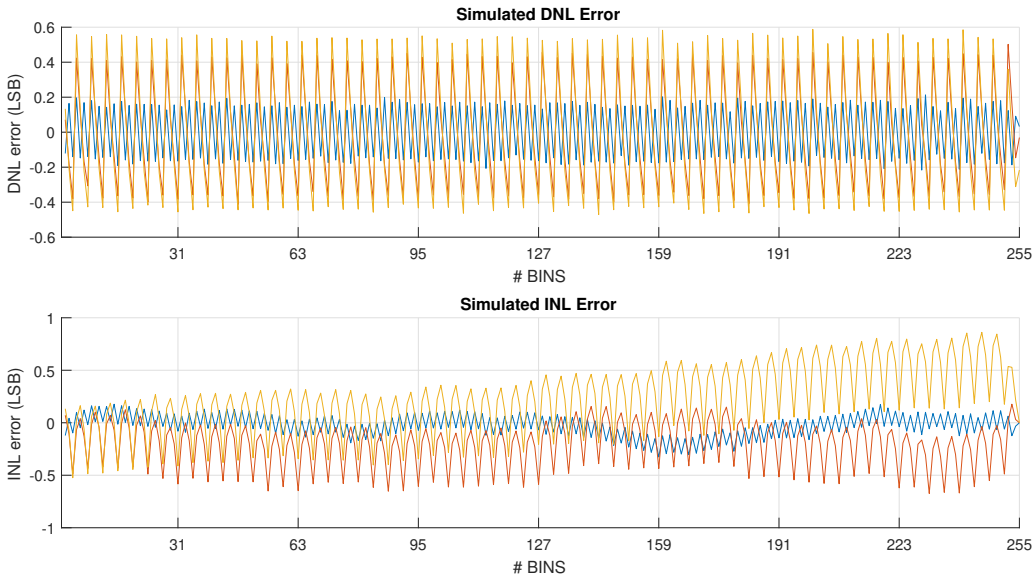

Figure 3: Simulated DNL and INL error of the interlocked interpolations technique compared to the regular technique.

The difference between the two regular interpolations is the delay buffer drive strength the red curve is representing the drive strength of only one delay buffer. The yellow curve is representing the results for double drive strength, comparable with the interlocked interpolation. What can be seen is that the DNL error of the regular interpolation with double the buffer drive strength has a larger DNL error compared to the smaller drive strength. This effect can be explained because for the same interpolation resistor the loading on the resistor chain also increases, which increases the delay error between the interpolation resistors around the delay buffer.

For the overall Non-linearity performance a monte-carlo analysis is performed over 100 samples. Here the maximum DNL and INL error are taken from every measurement and averaged. Table (1) shows the comparison of the monte carlo analysis of the three designs.

	Interlocked		Regular		Regular x2	
	M	SD	M	SD	M	SD
DNL (LSB)	0.216	0.008	0.526	0.026	0.587	0.010
INL (LSB)	0.306	0.061	0.818	0.127	0.960	0.064

Table 1:

5. Conclusion

In this paper a novel interpolation technique is presented. Simulation results prove that this interlocked interpolation technique reduces the INL/DNL error while simplifying the layout. The presented novelty is implemented in a delay line based time to digital converter which is placed inside a DLL to compensate for PVT and TID variations. The TDC achieves a resolution of 4 ps with an INL of 0.3 LSB which is significantly better compared to the regular interpolation technique.

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